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September 23, 2019

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Cards Against Confusion

Transient Execution
Tree v1.1.0b
(RDCT/LPFBSDFT)

A man with dark hair and a beard, wearing a blue long-sleeved shirt, is sitting on a black metal chair at a black table outdoors. He is holding a black mug. On the table in front of him are several items: a black mug, a microphone on a stand, and some papers. A white sign is attached to the front of the table with black text. The sign reads "side channel = obtaining meta-data and deriving secrets from it" and "CHANGE MY MIND" below a horizontal line. The setting is a brick-paved area with trees and a building in the background.

side channel
= obtaining meta-data and
deriving secrets from it

CHANGE MY MIND

Intel Analysis of Speculative Execution Side Channels

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1 of 12



100%



Intel Analysis of Speculative Execution Side Channels

[White Paper](#)



Spectre v1,



Spectre v1, Spectre v2,



Spectre v1, Spectre v2, Meltdown,



Spectre v1, Spectre v2, Meltdown, Spectre v3,



Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP,



Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP, Spectre v3.1,



Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP, Spectre v3.1, Foreshadow,



Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP, Spectre v3.1, Foreshadow, Foreshadow-NG,



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Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP, Spectre v3.1, Foreshadow, Foreshadow-NG, L1TF, Spectre v1.1, Spectre v4,



Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP, Spectre v3.1, Foreshadow, Foreshadow-NG, L1TF, Spectre v1.1, Spectre v4, SpectreRSB,



Spectre v1, Spectre v2, Meltdown, Spectre v3, LazyFP, Spectre v3.1, Foreshadow, Foreshadow-NG, L1TF, Spectre v1.1, Spectre v4, SpectreRSB, ret2spec,



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I guess I missed a few...?





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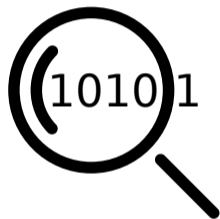
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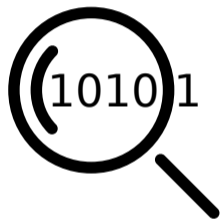


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- clear difference in behavior







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→ You directly read the value. This is not side channels.



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SPECTRE

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- Exploit control (or data) **flow predictions**



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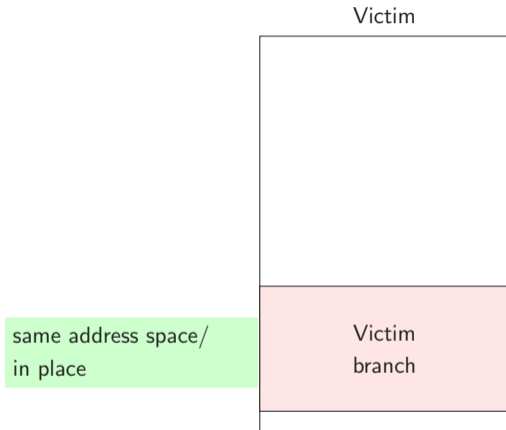
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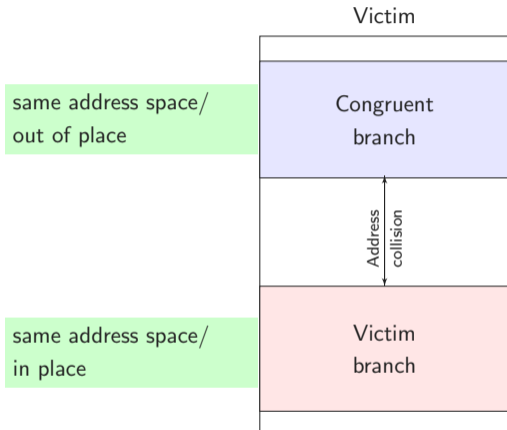


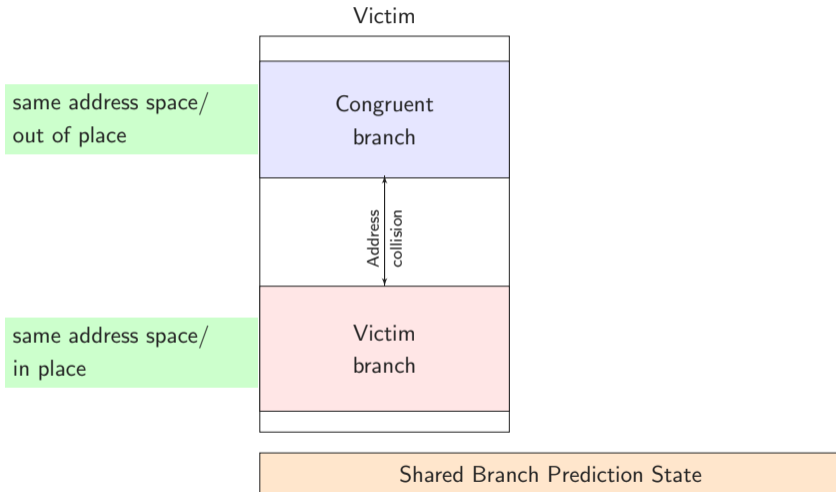
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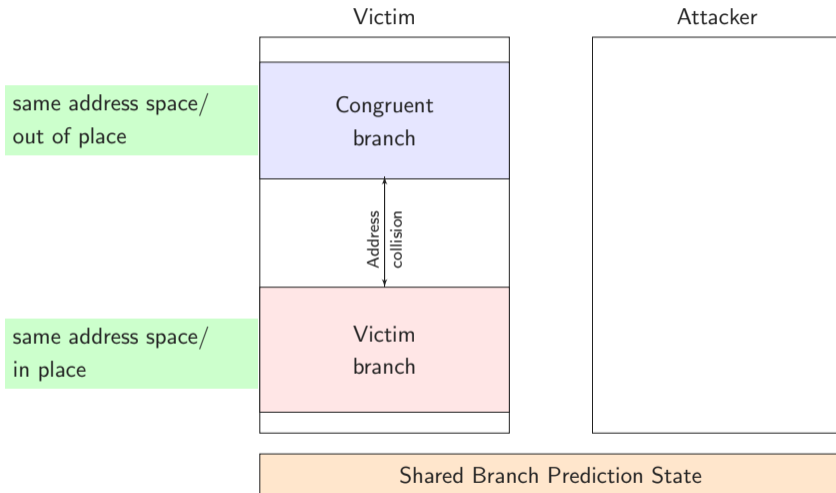


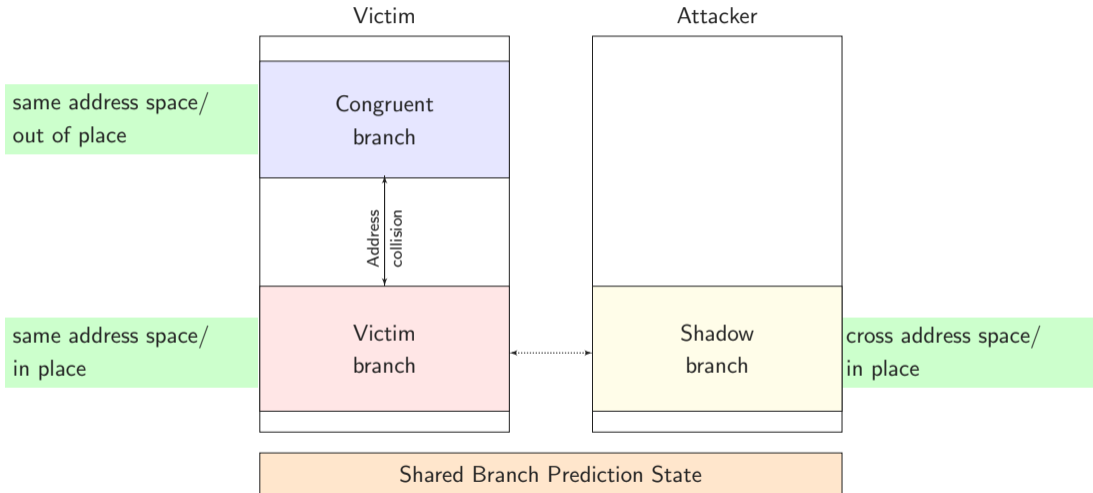
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- Most are even **shared** among processes

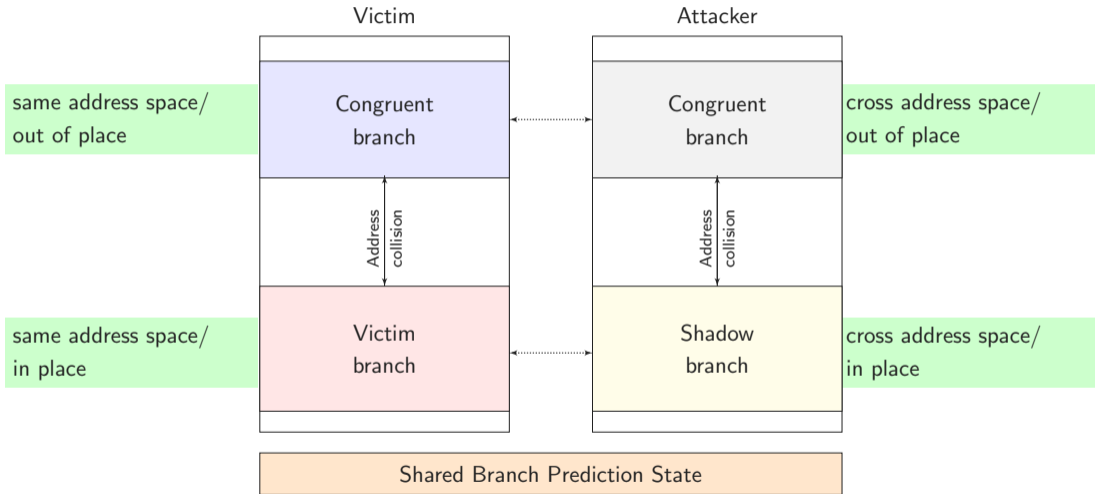




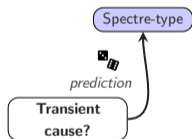


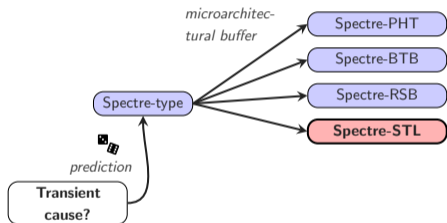


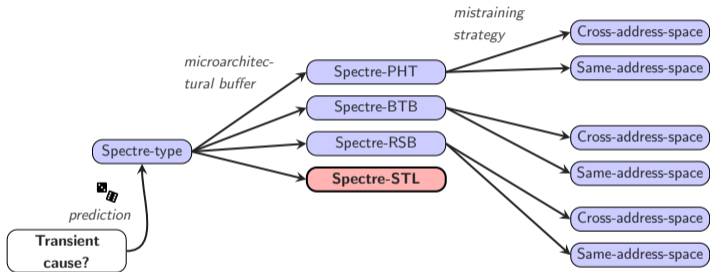


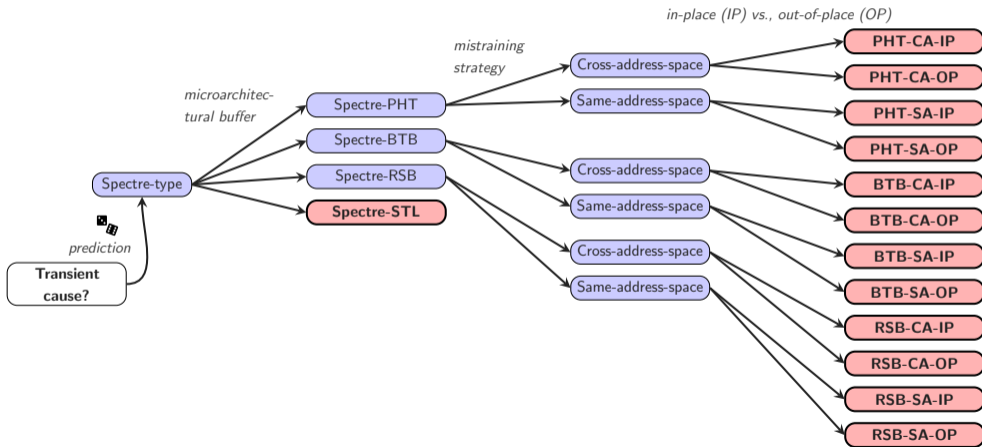


Transient
cause?











MELTDOWN

- **Meltdown** is a separate class of transient execution attack



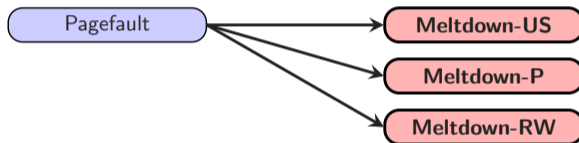
MELTDOWN

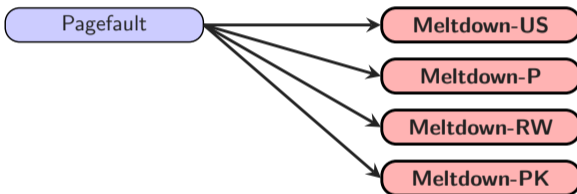
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- Exploit **lazy fault handling**

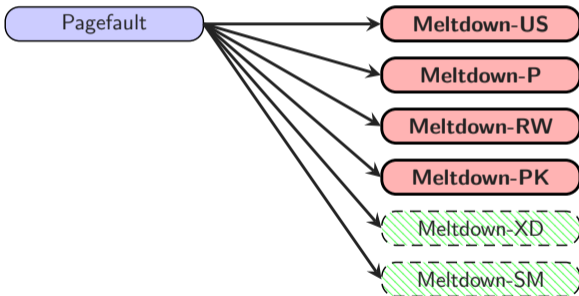
Pagefault



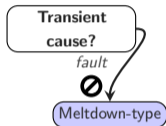


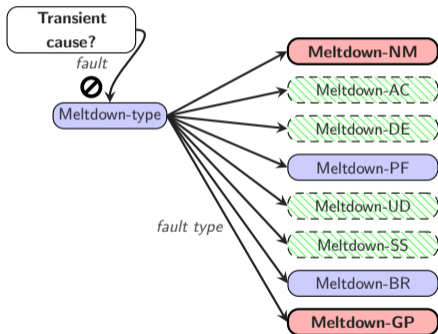


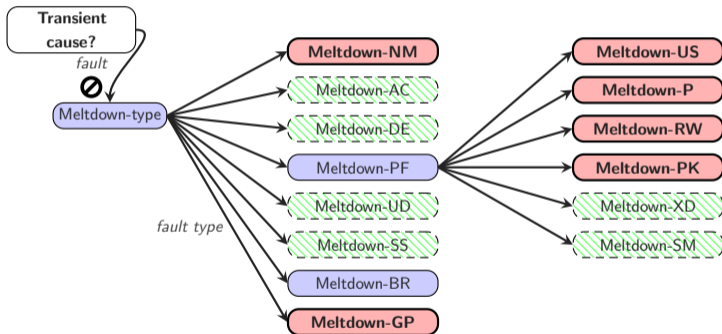


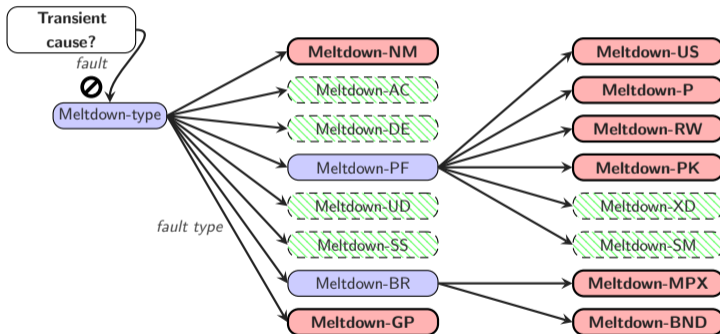


Transient
cause?









Meltdown Redux: Intel Flaw Lets Hackers Siphon Secrets from Millions of PCs

Two different groups of researchers found another speculative execution attack that can steal all the data a CPU touches.

ars TECHNICA

BIZ & IT TECH SCIENCE POLICY CARS GAMING & CULTURE STORE

I SPECULATE THAT THIS WON'T BE THE LAST SUCH BUG —

New speculative execution bug leaks data from Intel chips' internal buffers

Intel-specific vulnerability was found by researchers both inside and outside the company.



- May 2019: 3 new **Meltdown-type** attacks
- Leakage from: line-fill buffer, store buffer, load ports





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- Key take-aways:
 1. Leakage from **intermediate buffers** (\supset L1D)
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⇒ **How to classify in our tree + lessons learned?**

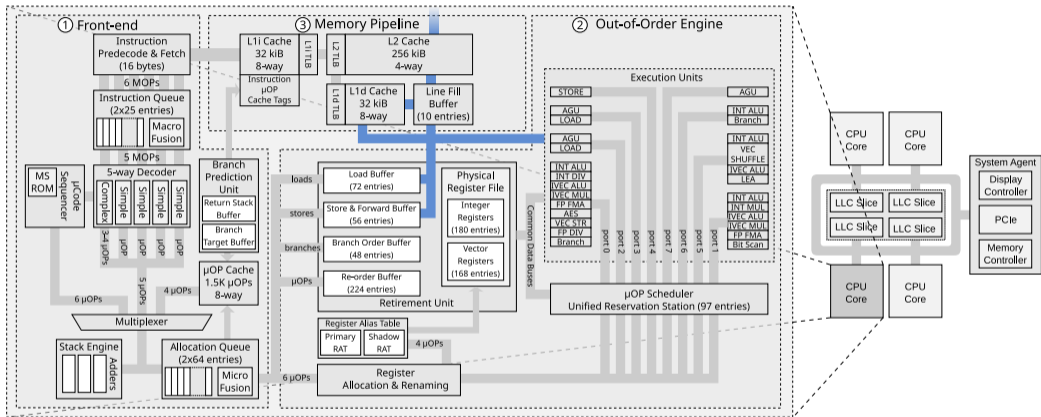


Figure 1: by Stephan van Schaik (<https://mdsattacks.com/>).



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- More complex edge cases (slow-path) in **microcode**



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- Optimization: only implement fast-path in **silicon**
- More complex edge cases (slow-path) in **microcode**
- Need help? Re-issue the load with a **microcode assist**
 - assist == “microarchitectural fault”
- Example: setting A/D bits in the page table walk
 - Likely many more!



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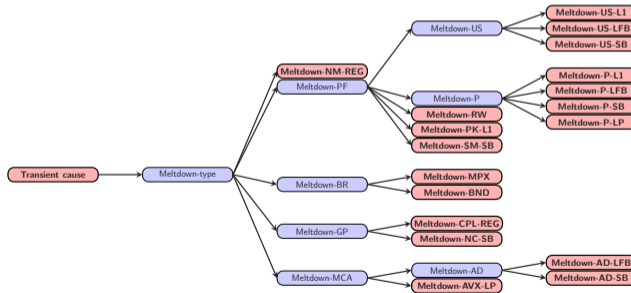
Add sub-branch – trigger Meltdown via μ -code assists

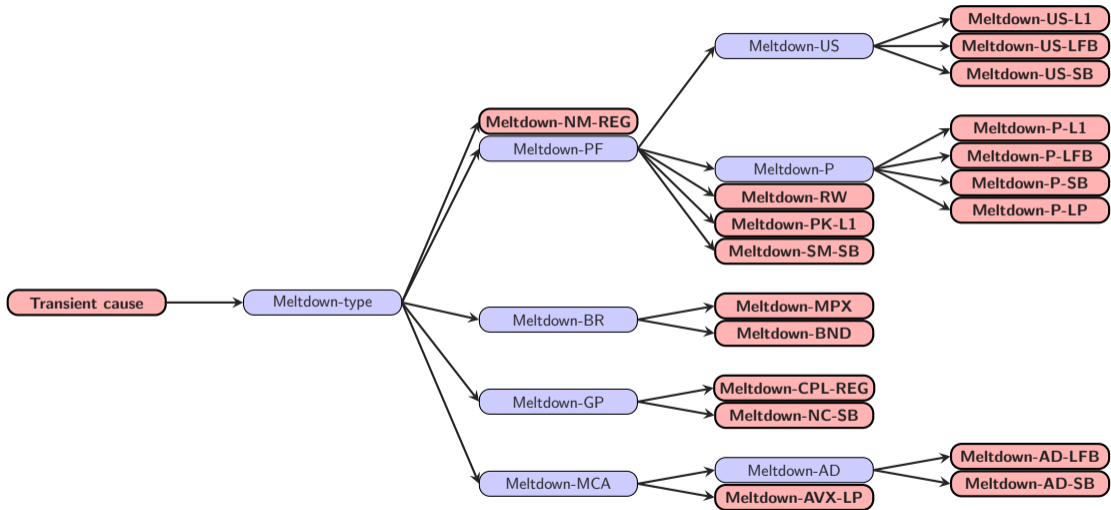


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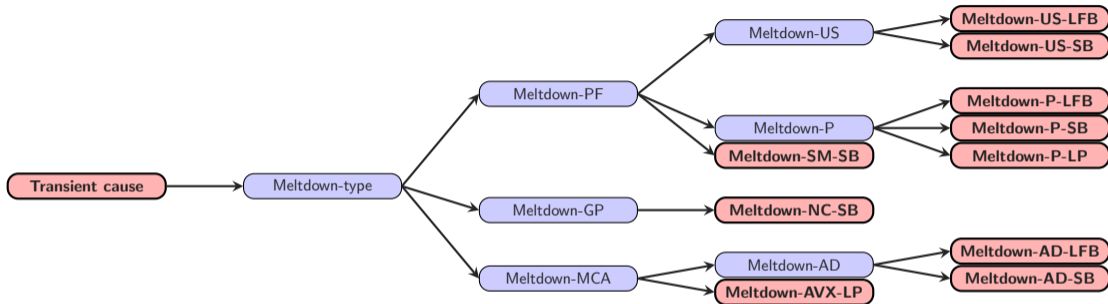




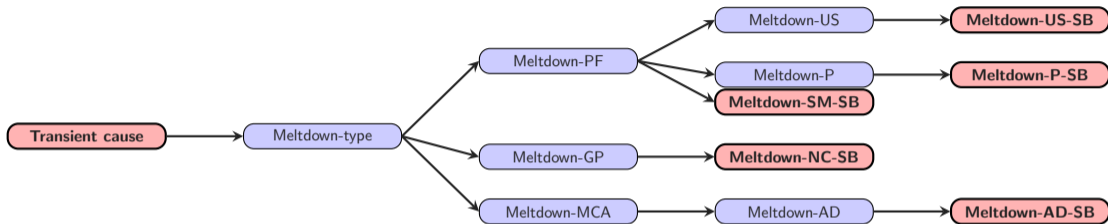




⇒ Our **systematic analysis** (tree search) revealed several overlooked variants (see Canella et al. “A Systematic Evaluation of Transient Execution Attacks and Defenses”, USENIX Security 2019).



Explore leakage from new **buffers** + microcode **assists**



Not “just another buffer”, include systematic **fault type analysis**



- Collect information record for each attack:
 - Academic paper references
 - Naming aliases and CVEs
 - Affected vendors (Intel, AMD, ARM)
 - Open-source PoCs
- **Filter** by type, vendor, buffer, etc. → understand and build insights
- TikZ/SVG export
- Pull requests welcome! :-)

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