

Microarchitectural Attacks:

From the Basics to Arbitrary Read and Write Primitives without any Software Bugs

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June 19, 2018

Graz University of Technology





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FOOD CACHE

Revolutionary concept!

Store your food at home, never go to the grocery store during cooking.

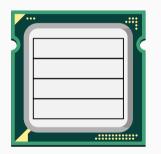
Can store **ALL** kinds of food.

ONLY TODAY INSTEAD OF \$1,300



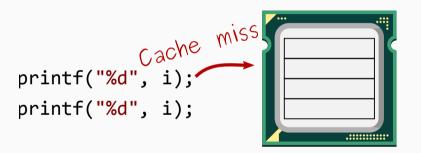
ORDER VIA PHONE: +555 12345

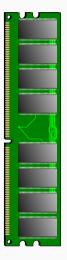


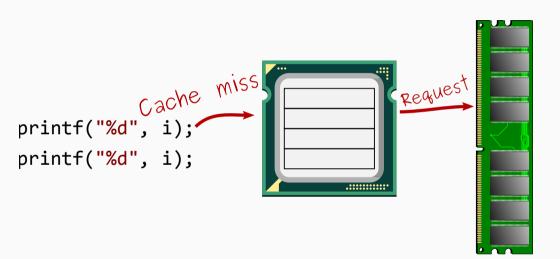


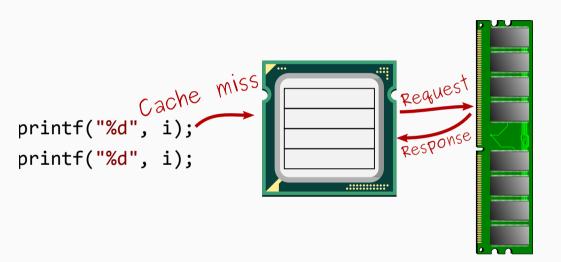
printf("%d", i); printf("%d", i);

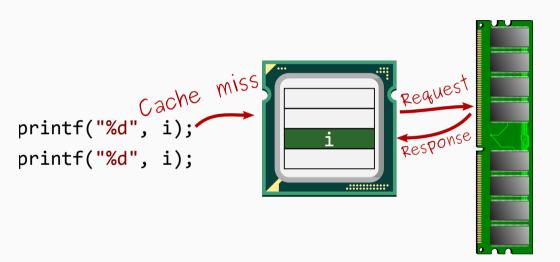


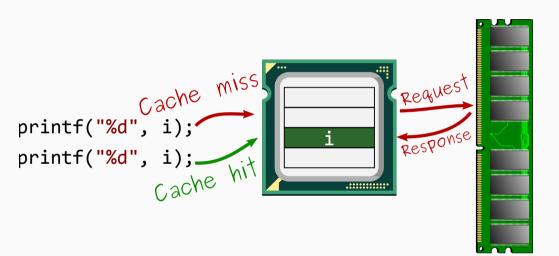




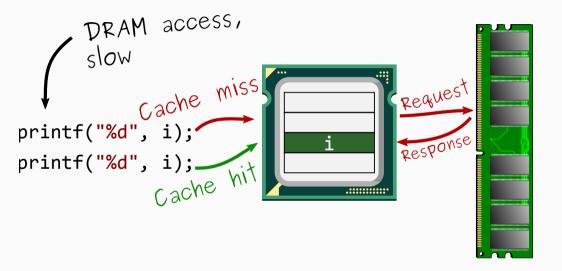




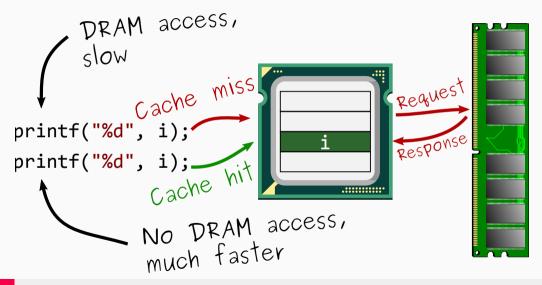


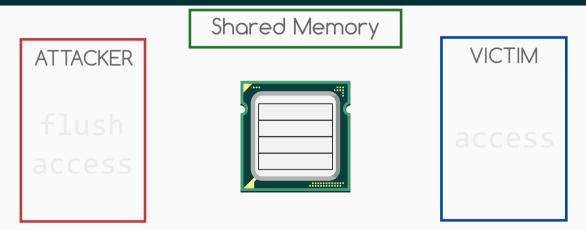


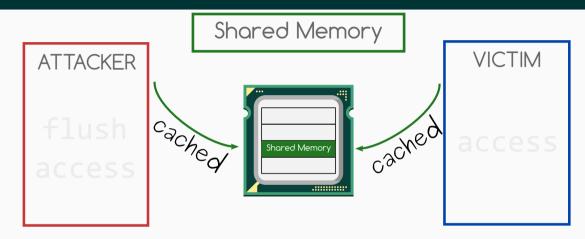
CPU Cache

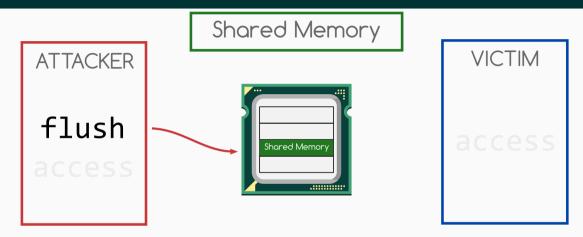


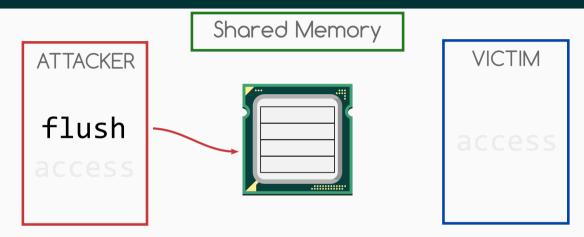
CPU Cache

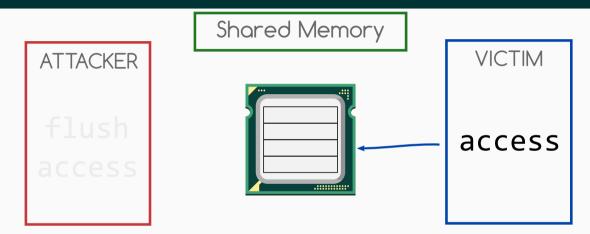


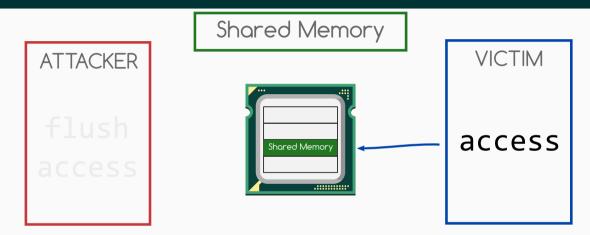


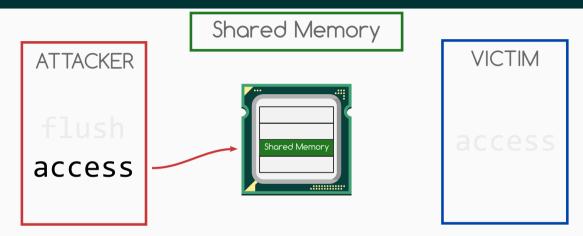


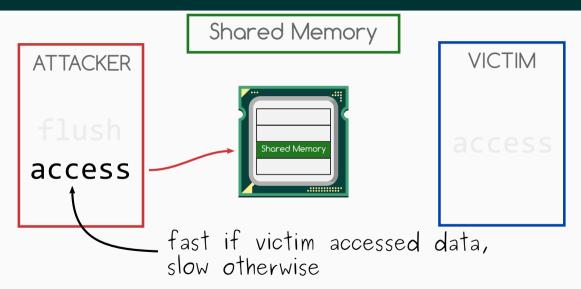


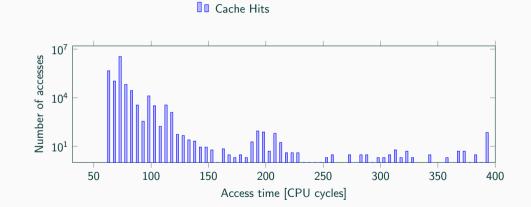




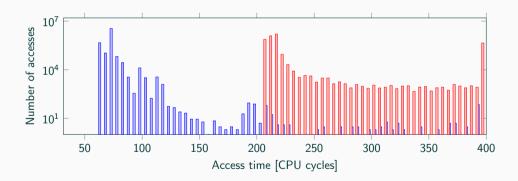








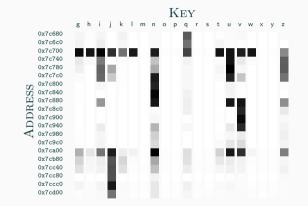
Cache Hits Cache Misses



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Cache Template Attack Demo

Cache Template



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7





7. Serve with cooked and peeled potatoes





Wait for an hour



Wait for an hour

LATENCY

1. Wash and cut vegetables

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

4. Fry vegetables until golden and softened



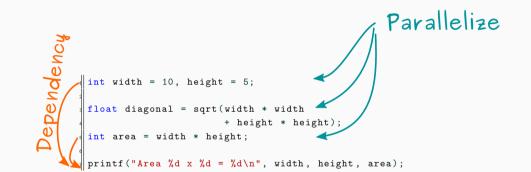
1. Wash and cut vegetables

Parallelize

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

4. Fry vegetables until golden and softened







segfault at ffffffff81a000e0 ip 000000000400535
sp 00007ffce4a80610 error 5 in reader



segfault at ffffffff81a000e0 ip 000000000400535 sp 00007ffce4a80610 error 5 in reader

• Kernel addresses are not accessible



segfault at ffffffff81a000e0 ip 000000000400535 sp 00007ffce4a80610 error 5 in reader

- Kernel addresses are not accessible
- Are privilege checks also done when executing instructions out of order?

• Adapted code



```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

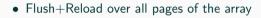
• Adapted code

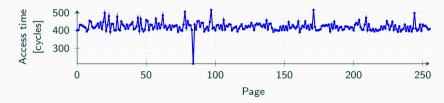


```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

• Static code analyzer is not happy

1 warning: Dereference of null pointer
2 *(volatile char*)0;

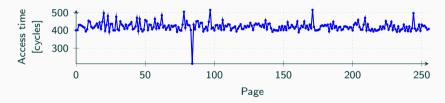




• "Unreachable" code line was actually executed



• Flush+Reload over all pages of the array



- "Unreachable" code line was actually executed
- Exception was only thrown afterwards





• Combine the two things

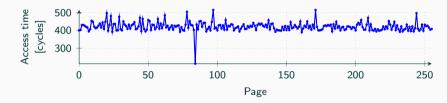


• Combine the two things

• Then check whether any part of array is cached



 $\bullet~\mbox{Flush+Reload}$ over all pages of the array



• Index of cache hit reveals data

• Flush+Reload over all pages of the array





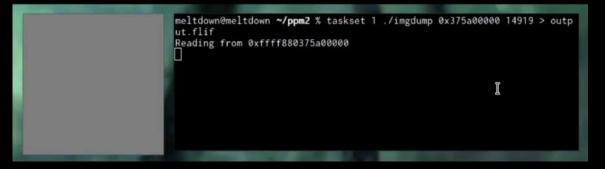
- Index of cache hit reveals data
- Permission check is in some cases not fast enough

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U	nlock

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CAN YOU ENHANCE THAT



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		-	f94b7840: 69 63 6f 6e 73 2f 33 35 34 2f 33 35 34 33 39 39 icons/354
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		- 1	f94b7860: 3d 31 34 35 32 32 34 34 38 31 35 XX XX XX XX =14522448

How to mitigate Meltdown?

• Kernel addresses in user space are a problem

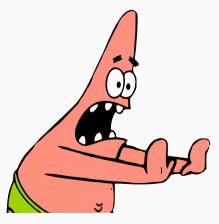
- Kernel addresses in user space are a problem
- Why don't we take the kernel addresses...







• ...and remove them if not needed?

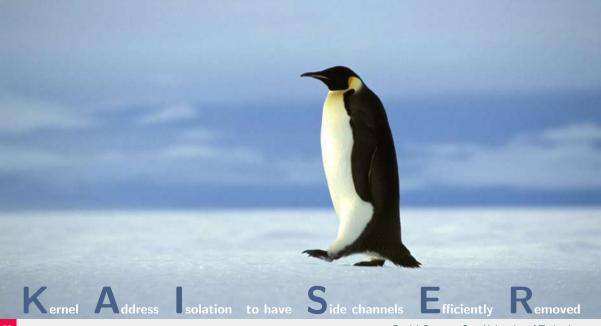


- ...and remove them if not needed?
- User accessible check in hardware is not reliable

CAN'T LEAK DATA

IF THERE IS NO DATA



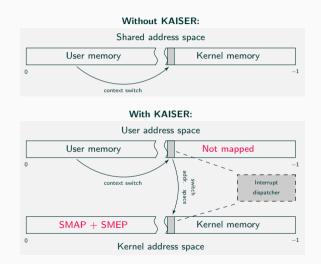


KAISER /'kAIzə/ 1. [german] Emperor, ruler of an empire 2. largest penguin, emperor penguin



Removed

Address Isolation to have Side channels Efficiently





• We published KAISER in July 2017



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- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)



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- Microsoft implemented similar concept in Windows 10



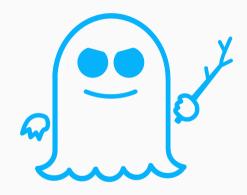
- We published KAISER in July 2017
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it "Double Map"



- We published KAISER in July 2017
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it "Double Map"
- All share the same idea: switching address spaces on context switch

Meltdown and Spectre







Meltdown and Spectre





SPECTRE



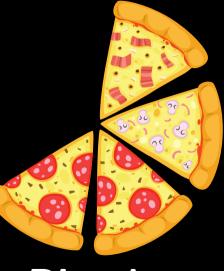


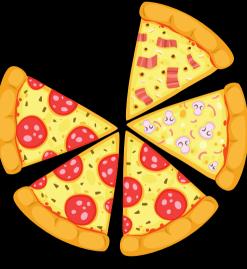
Prosciutto



Funghi













Speculative Cooking













• Mistrains branch prediction



- Mistrains branch prediction
- CPU speculatively executes code which should not be executed



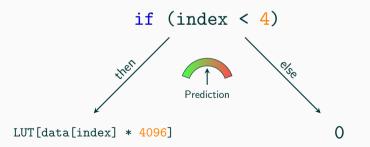
- Mistrains branch prediction
- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls

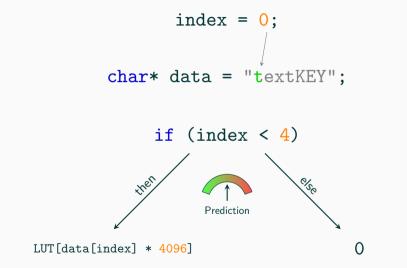


- Mistrains branch prediction
- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls
- $\rightarrow\,$ Spectre "convinces" program to execute code

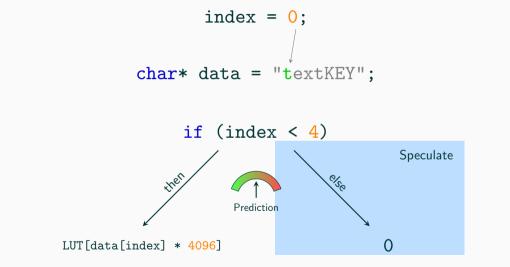


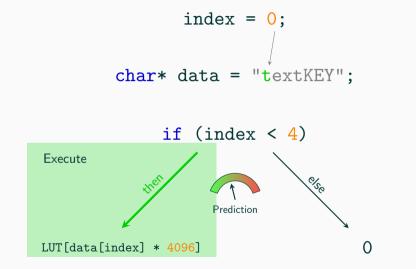
index =
$$0;$$





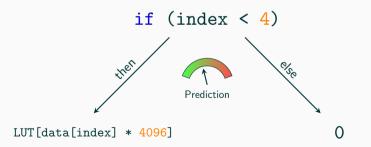
Spectre (variant 1)

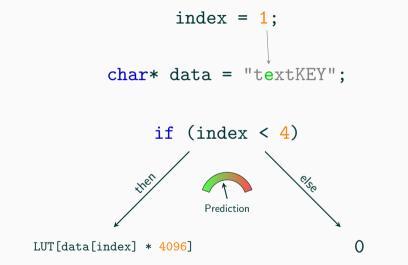




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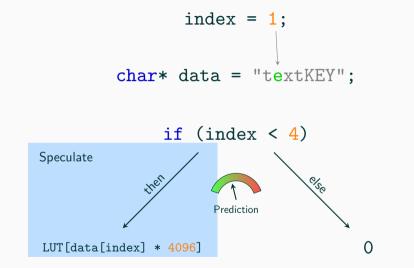
index =
$$1;$$

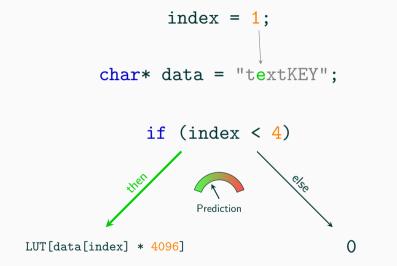




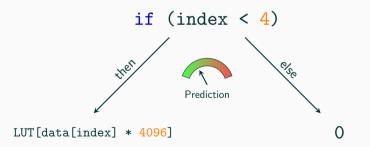
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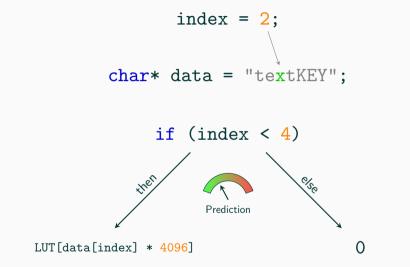
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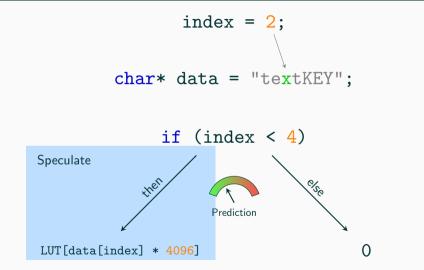


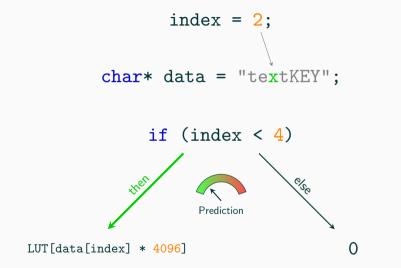


index =
$$2;$$

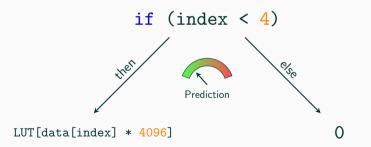


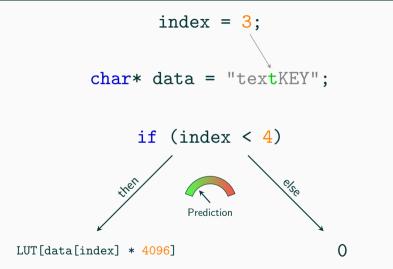


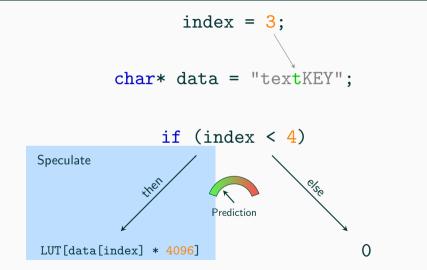


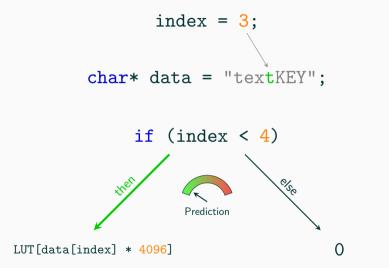


index =
$$3;$$

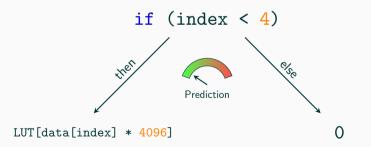


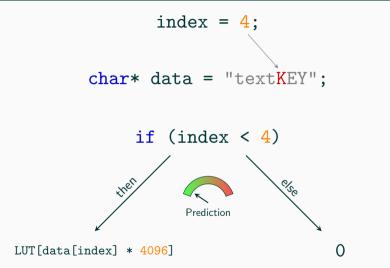


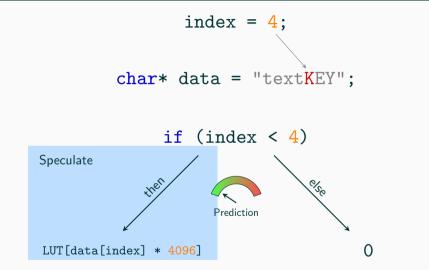


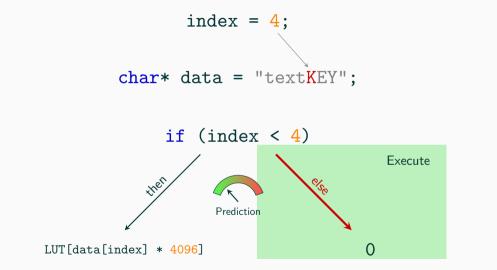


index =
$$4;$$

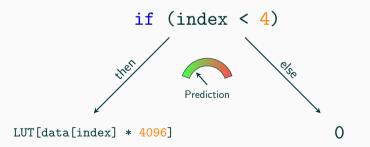






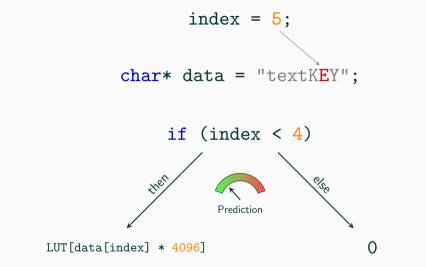


index =
$$5;$$



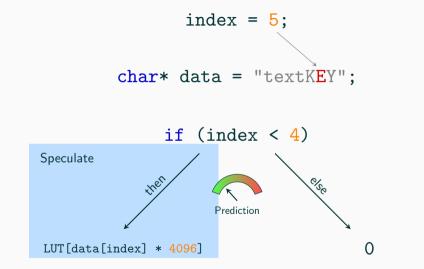
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Spectre (variant 1)

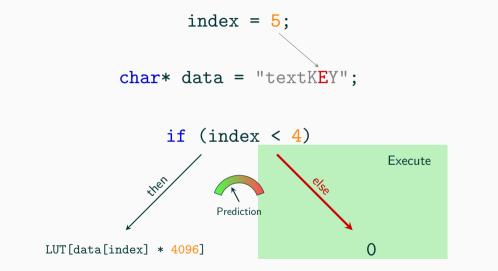


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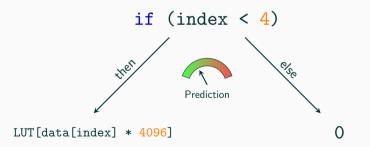
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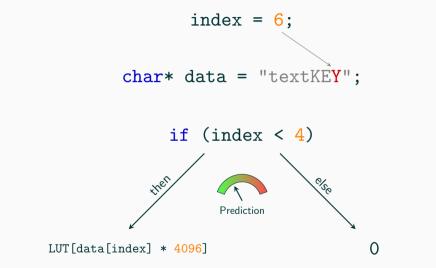


index =
$$6;$$

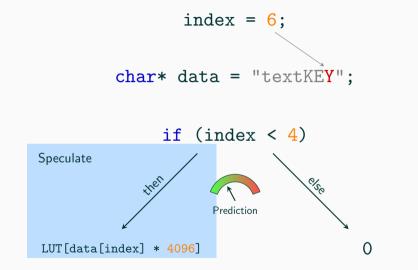


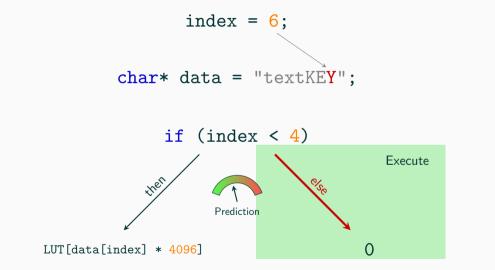
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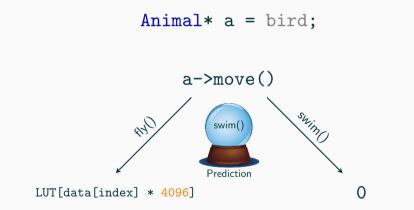
Spectre (variant 1)



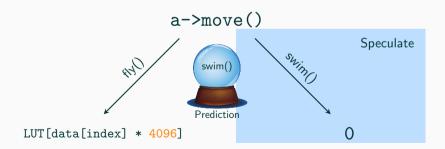
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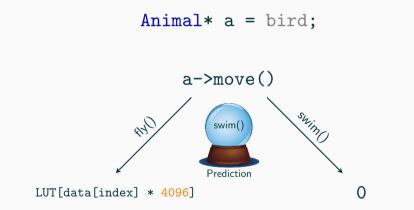


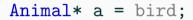


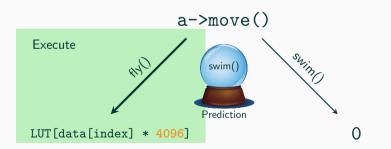


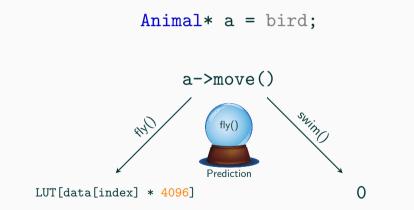
Animal* a = bird;



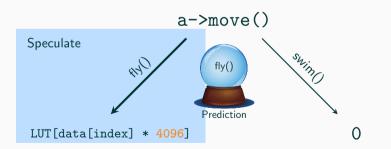


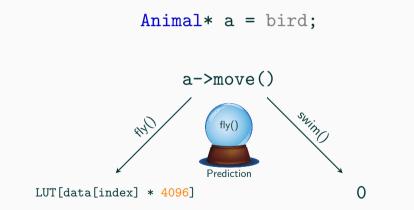


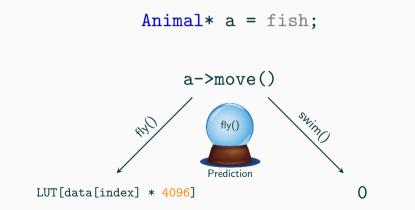




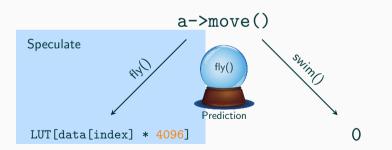


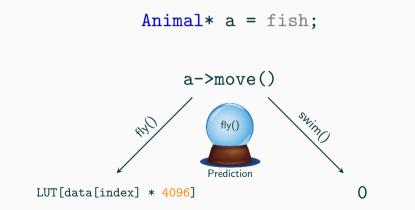




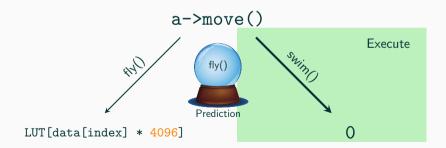


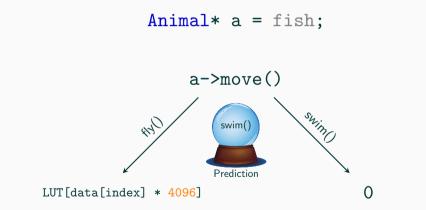






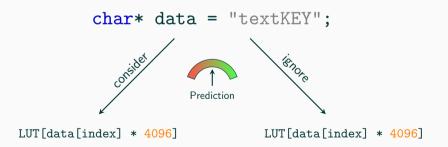
Animal* a = fish;

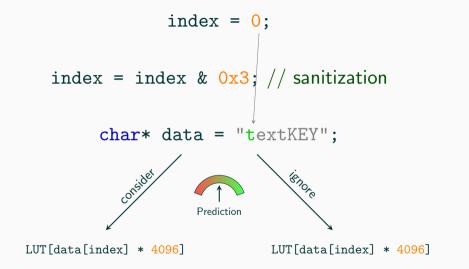


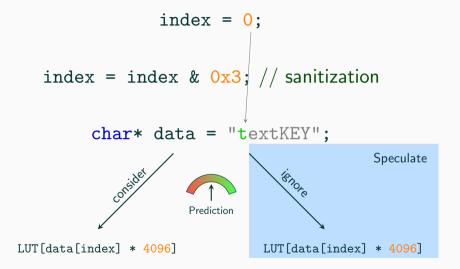


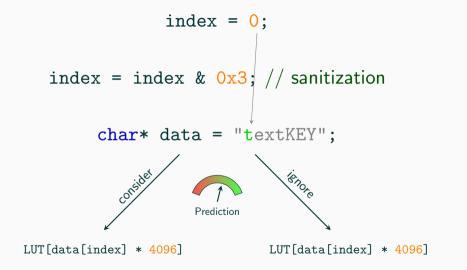
index =
$$0;$$

index = index &
$$0x3$$
; // sanitization



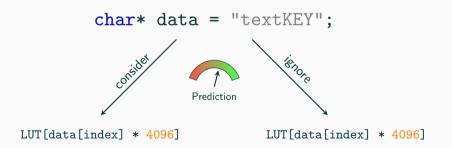


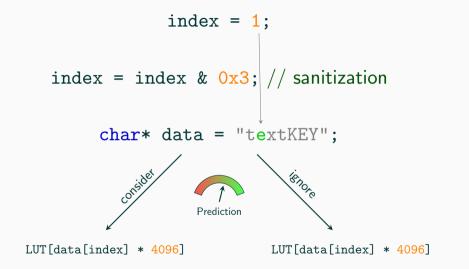


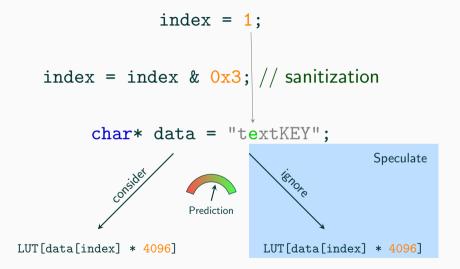


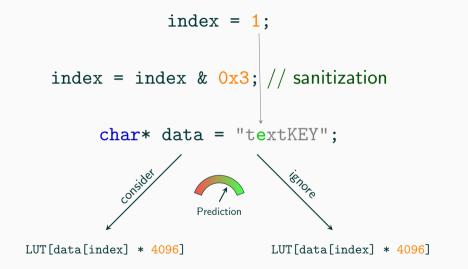
index = 1;

index = index & 0x3; // sanitization



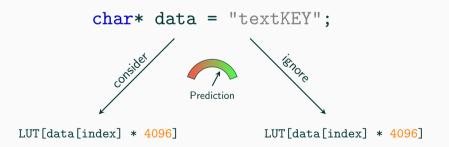


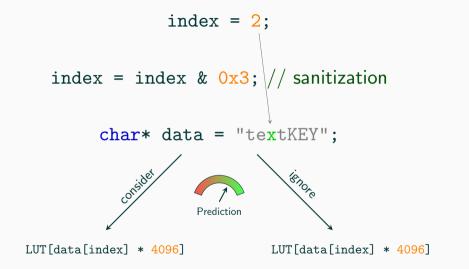


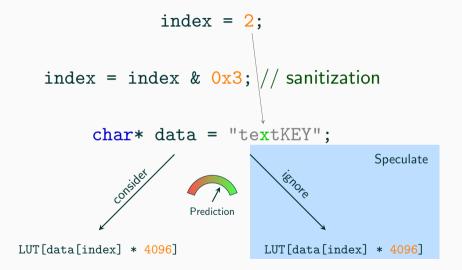


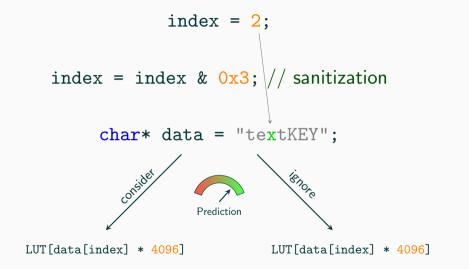
index =
$$2;$$

index = index &
$$0x3$$
; // sanitization



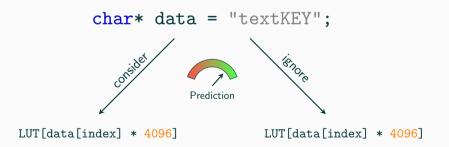


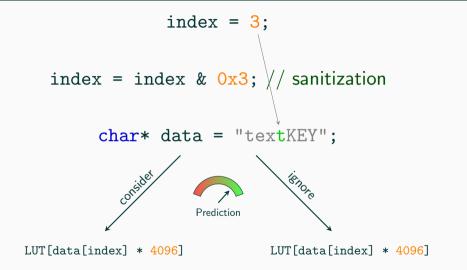


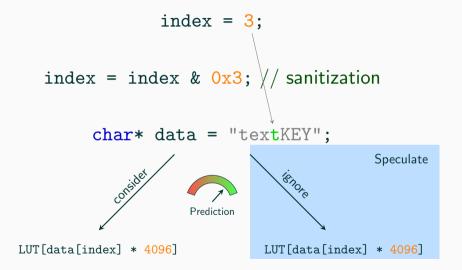


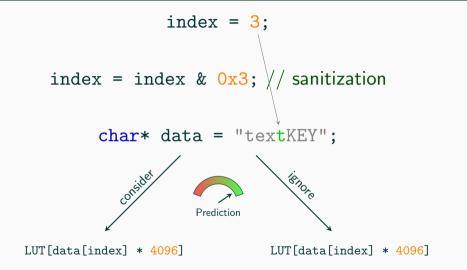
index =
$$3;$$

index = index &
$$0x3$$
; // sanitization



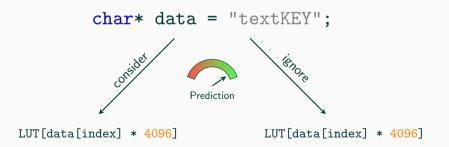


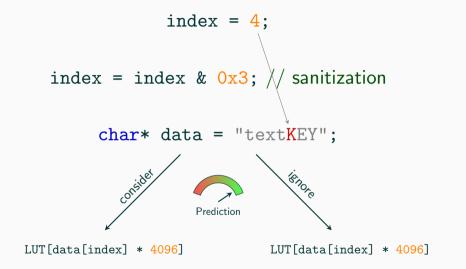


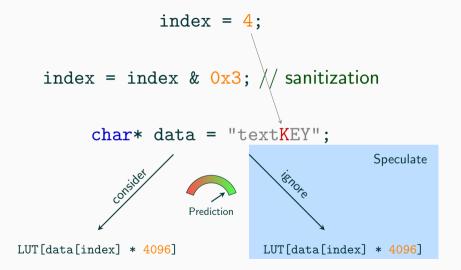


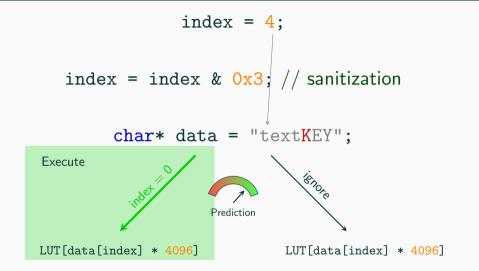
index =
$$4;$$

index = index &
$$0x3$$
; // sanitization



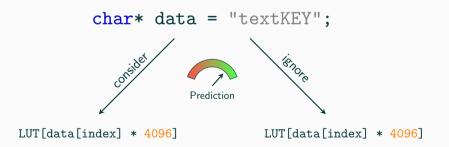


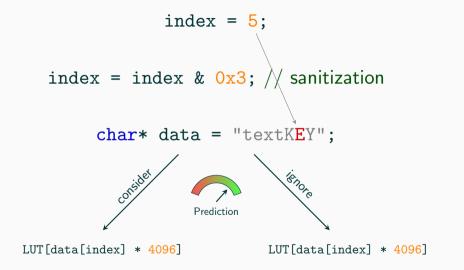




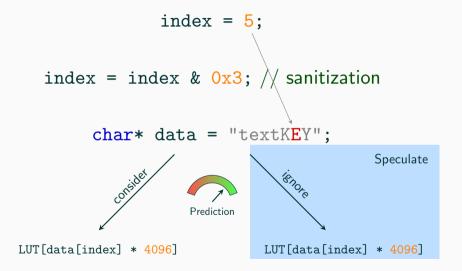
index =
$$5;$$

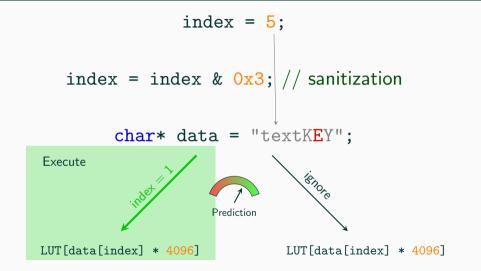
index = index &
$$0x3$$
; // sanitization





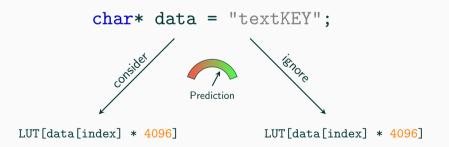
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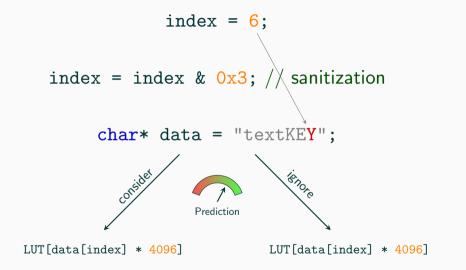


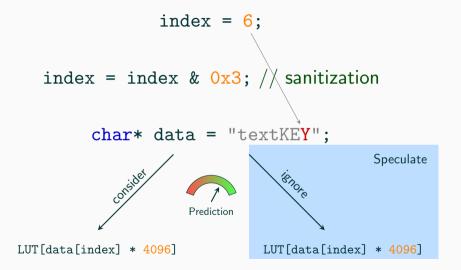


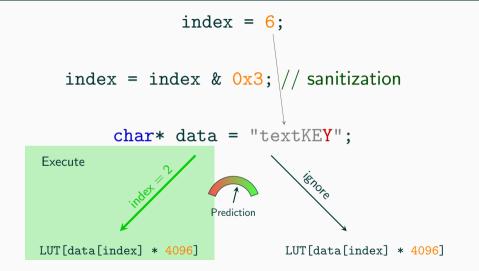
index =
$$6;$$

index = index &
$$0x3$$
; // sanitization











• Trivial approach: disable speculative execution



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- No wrong speculation if there is no speculation



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- No wrong speculation if there is no speculation
- Problem: massive performance hit!



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- Also: How to disable it?



- Trivial approach: disable speculative execution
- No wrong speculation if there is no speculation
- Problem: massive performance hit!
- Also: How to disable it?
- Speculative execution is deeply integrated into CPU





• Workaround: insert instructions stopping speculation



- Workaround: insert instructions stopping speculation
- $\rightarrow\,$ insert after every bounds check



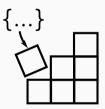


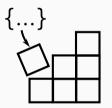
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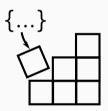


- Workaround: insert instructions stopping speculation
- $\rightarrow\,$ insert after every bounds check
 - ×86: LFENCE, ARM: CSDB
 - Available on all Intel CPUs, retrofitted to existing ARMv7 and ARMv8

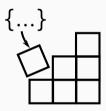




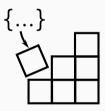
• Speculation barrier requires compiler supported



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- Already implemented in GCC, LLVM, and MSVC



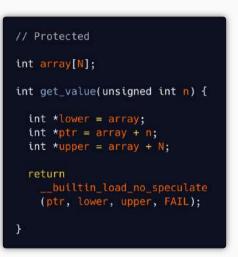
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- Speculation barrier requires compiler supported
- Already implemented in GCC, LLVM, and MSVC
- Can be automated (MSVC) \rightarrow not really reliable
- Explicit use by programmer: __builtin_load_no_speculate

```
// Unprotected
int array[N];
int get_value(unsigned int n) {
  int tmp;
  if (n < N) {
    tmp = array[n]
  } else {
    tmp = FAIL;
  }
  return tmp;
}
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• Speculation barrier works if affected code constructs are known



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- Programmer has to fully understand vulnerability



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- Automatic detection is not reliable





- Speculation barrier works if affected code constructs are known
- Programmer has to fully understand vulnerability
- Automatic detection is not reliable
- Non-negligible performance overhead of barriers

Intel released microcode updates

• Indirect Branch Restricted Speculation (IBRS):

୦-I-୦-I-୦ I-୦-I-୦-I ୦-I-୦-I-୦ I-୦-I-୦-I

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 - Do not speculate based on anything before entering IBRS mode

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- Indirect Branch Restricted Speculation (IBRS):
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 - $\rightarrow\,$ lesser privileged code cannot influence predictions

୦-I-୦-I-୦ I-୦-I-୦-I ୦-I-୦-I-୦ I-୦-I-୦-I

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- Indirect Branch Predictor Barrier (IBPB):

୦-I-୦-I-୦ I-୦-I-୦-I ୦-I-୦-I-୦ I-୦-I-୦-I

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 - Flush branch-target buffer

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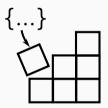
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- Single Thread Indirect Branch Predictors (STIBP):

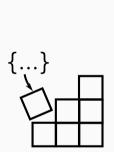
0-1-0-1-0 1-0-1-0-1 0-1-0-1-0 1-0-1-0-1

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- Single Thread Indirect Branch Predictors (STIBP):
 - Isolates branch prediction state between two hyperthreads

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0-1-0-1-0 1-0-1-0-1 0-1-0-1-0 1-0-1-0-1 Retpoline (compiler extension)

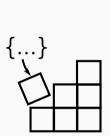




```
Retpoline (compiler extension)
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push <call_target>
call 1f
2: ; speculation will continue here
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jmp 2b ; endless loop
1:
lea 8(%rsp), %rsp ; restore stack pointer
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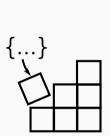
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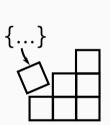
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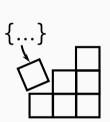
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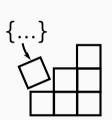
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- $\rightarrow\,$ always predict to enter an endless loop
- instead of the correct (or wrong) target function \rightarrow performance?
- On Broadwell or newer:
 - ret may fall-back to the BTB for prediction
 - $\rightarrow\,$ microcode patches to prevent that



• ARM provides hardened Linux kernel

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- Clears branch-predictor state on context switch



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- Either via instruction (BPIALL)...



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- ...or workaround (disable/enable MMU)



- ARM provides hardened Linux kernel
- Clears branch-predictor state on context switch
- Either via instruction (BPIALL)...
- ...or workaround (disable/enable MMU)
- Non-negligible performance overhead (\approx 200-300 ns)

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Intel released microcode updates

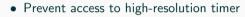
0-1-0-1-0 1-0-1-0-1 0-1-0-1-0 1-0-1-0-1

Intel released microcode updates

- Disable store-to-load-forward speculation
- Performance impact of 2-8%

• Prevent access to high-resolution timer





 $\rightarrow~\mbox{Own}$ timer using timing thread





- Prevent access to high-resolution timer
- $\rightarrow~{\rm Own}$ timer using timing thread
- Flush instruction only privileged



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- $\rightarrow~{\rm Own}$ timer using timing thread
 - Flush instruction only privileged
- $\rightarrow\,$ Cache eviction through memory accesses
- Just move secrets into secure world
- $\rightarrow\,$ Spectre works on secure enclaves



• Out-of-Order Execution

Spectre

• Speculative Execution (subset of Out-of-Order Execution)

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- has nothing to do with branch prediction

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- mitigated by KAISER

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Spectre

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Meltdown

- performs illegal memory accesses \rightarrow we need to take care of processor exceptions
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 - $\bullet\,$ exception suppression with TSX

Spectre

- performs only legal memory accesses
 - has nothing to do with exception handling or suppression

Meltdown

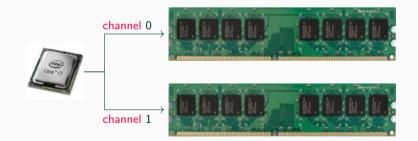
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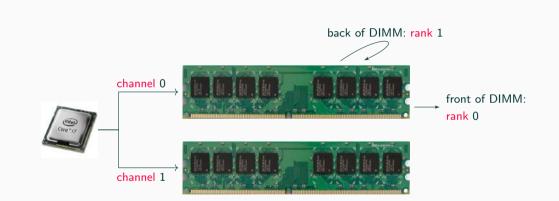
Spectre

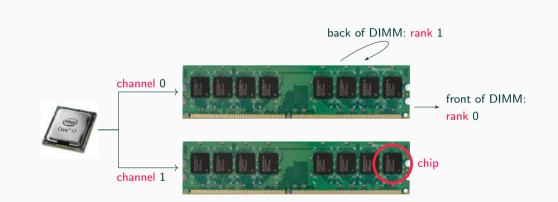
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What if we want to modify data?

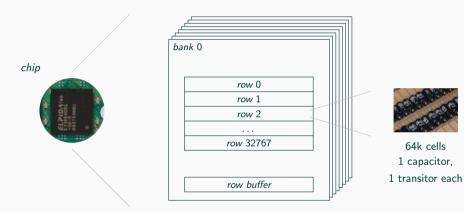


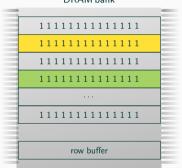




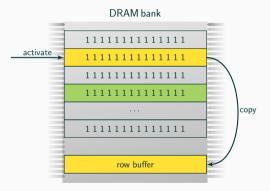




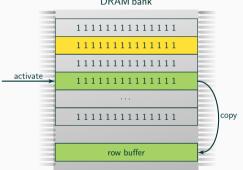




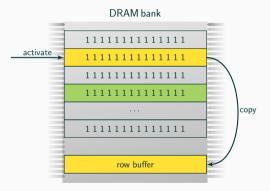
- Cells leak \rightarrow repetitive refresh necessary
- Maximum interval between refreshes to guarantee data integrity
- Cells leak faster upon proximate accesses \rightarrow Rowhammer



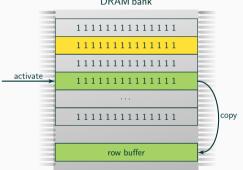
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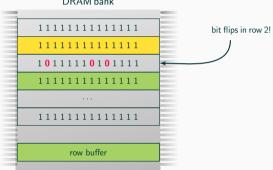
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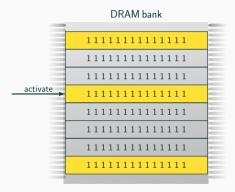
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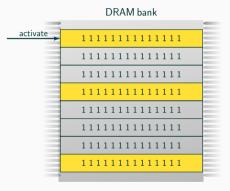
• There are two different hammering techniques

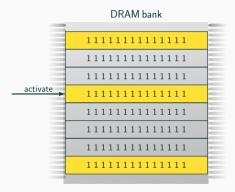
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- #1: Hammer one row next to victim row and other random rows

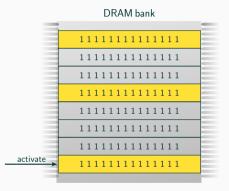
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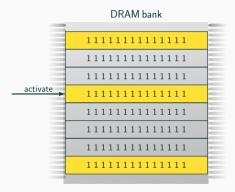
- There are three different hammering techniques
- #1: Hammer one row next to victim row and other random rows
- #2: Hammer two rows neighboring victim row
- #3: Hammer only one row next to victim row

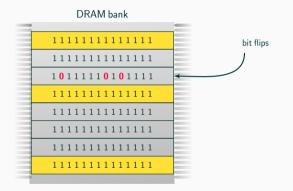


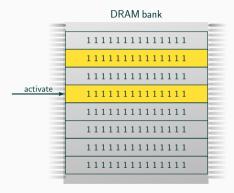


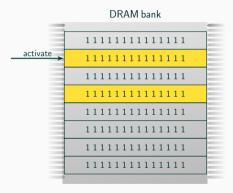


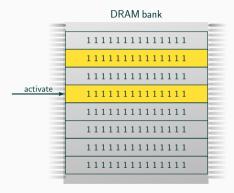


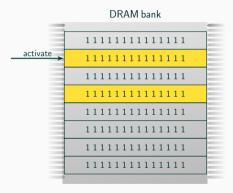


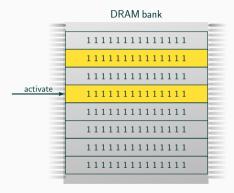


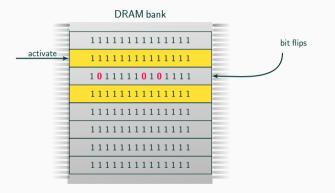


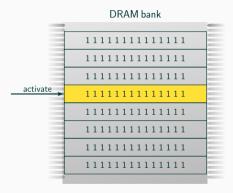






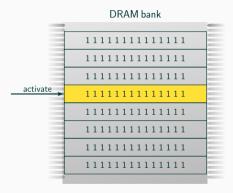






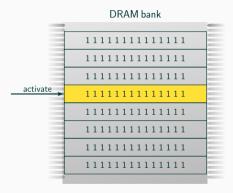
DRAM bank _

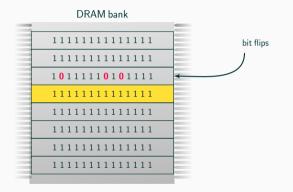
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DRAM bank _

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 - 4. Trigger bit flip again







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- They can be used by unprivileged users as well

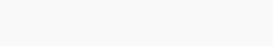


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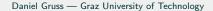
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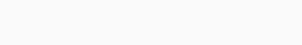


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 - $\rightarrow\,$ difficult to optimize with an intelligent adversary



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- $\rightarrow\,$ for years we solely optimized for performance



After learning about a side channel you realize:

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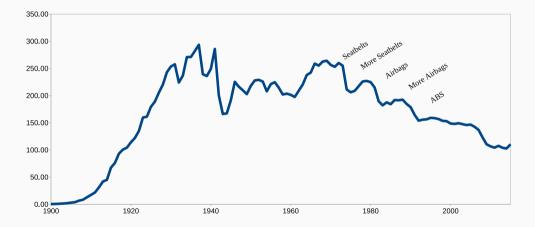
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After learning about a side channel you realize:

- the side channels were documented in the Intel manual
- only now we understand the implications



Motor Vehicle Deaths in U.S. by Year

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- moral obligation to invest more time on defenses than on attacks
- dangerous: we overlooked Meltdown and Spectre for decades
- we don't know all problems. do we know at least the most important subset?
- are we hammering on a small subset of problems and forgot about the bigger picture?



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A unique chance to

• rethink processor design



A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)



A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)
- dedicate more time into identifying problems and not solely in mitigating known problems



Microarchitectural Attacks:

From the Basics to Arbitrary Read and Write Primitives without any Software Bugs

Daniel Gruss

June 19, 2018

Graz University of Technology