

## Microarchitectural Attacks: Meltdown and Spectre

#### **Daniel Gruss**

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• it is in the news, all over the world









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- it is in the news, all over the world
- you get a Wikipedia article in multiple languages

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## Meltdown (security vulnerability)

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detein Tale

Behildown to a frantiviste vulnerability affecting trial ADI matroprocessant and some ARM-based neuroprocessors,<sup>110023</sup> 8 allows a regue process to read all memory, even when it is not authoritant to do so.

Moltober affects a wide range of systems. At the time of disclosure, this included all devices running any bot file most sector and pathent sensions of XOE,<sup>16</sup> (Linux<sup>1001</sup>), macOL<sup>10</sup> or Windows. Accordingly, many senses and closed senses were impacted.<sup>10</sup> Takan<sup>1001</sup>, as well as a potential majority of annual devices and estimated devices using ARM based processors (mobile devices, amart TVs and others), including in wide range of retearting equipment. A purely isoftware service contain the Moltober has been assessed as showing computers between 5 and 3D percent in centain specialized workloads.<sup>10</sup> although comparison responsible for activative sometion of the exploit are reporting monimal impact from general terchinant testing.<sup>26</sup>

Metaboles was insued a Contration Vehiclassifies and Expansive ED at CVE-2017. IOV-44. Also known as Progree Deta Cactre Coucli<sup>10</sup> in January 2018. It was thistoped in conjunction with another exploit, Spectre, with which it shares some, but not all characteristics. The Metabolic and Spectre extremibilities are considered "contemptic".



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Tools

Observer to Wheel sector

## Spectre (security vulnerability)

First Weipedia. the heat adoptionidia

Spectre is a understability that affects masters microprocessors that perform branch production.<sup>(10,000</sup> On most processors, the speculative execution resulting from a branch misprediction may leave observable side effects that may rewait private data to attacknes. For example, if the pattern of nemony accesses performed by much speculative execution depends on private cato, the resulting date of the dato cather constitution side channel through which are attacked may be able to extend infernation which the private data using a throng attack.<sup>(10,001)</sup>

Two Coverses Waharabilities and Esposes the related to Spectre, CVE-2017-01556 (bound sheet bysise) and CVE-2017-015919 (Invent target reactor), have been inwest <sup>17</sup> UT engines and for JavaScript were band valuestile. A website can read data stored in the involve for another website, or the bowen's memory band.<sup>(11)</sup>

Several processives to help protect to every computers and related devices from the Bipectra (and Mediativer) security varies addition have been published (MIXEPUIC) Spectra patches have been reported to algolicantly also down performance, sepecially on other computers, on the new RM persisten Comp platforms, benchmark performance chops of 3–14 percent have been measured.<sup>11</sup> Mediatives patches may also produces, performance issue<sup>100,00</sup> Or January 16, 2018, univerted relations, even for investigation patches may also produce performance issue<sup>100,00</sup> Or January 16, 2018, univerted relations, even for investigations of the loss of the loss of the second second



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- you get a Wikipedia article in multiple languages
- there are comics, including xkcd





Come (Strip 2009)

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- you get a Wikipedia article in multiple languages
- there are comics, including xkcd
- you get a lot of Twitter follower after Snowden mentioned you



## The Wall









- Kernel is isolated from user space
- This isolation is a combination of hardware and software



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- User applications cannot access anything from the kernel



- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel
- There is only a well-defined interface → syscalls





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## 1337 4242 FOOD CACHE

#### Revolutionary concept!

Store your food at home, never go to the grocery store during cooking.

Can store **ALL** kinds of food.

ONLY TODAY INSTEAD OF \$1,300



ORDER VIA PHONE: +555 12345



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# printf("%d", i); printf("%d", i);







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CPU Cache



**CPU** Cache



### Flush+Reload




















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Cache Template Attack Demo

### **Cache Template**







7. Serve with cooked and peeled potatoes





### Wait for an hour



### Wait for an hour

# LATENCY

1. Wash and cut vegetables 2. Pick the basil leaves and set aside 3. Heat 2 tablespoons of oil in a pan 4. Fry vegetables until golden and softened



## 1. Wash and cut vegetables

### Parallelize

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

4. Fry vegetables until golden and softened







segfault at ffffffff81a000e0 ip 000000000400535
sp 00007ffce4a80610 error 5 in reader



segfault at ffffffff81a000e0 ip 0000000000400535 sp 00007ffce4a80610 error 5 in reader

• Kernel addresses are not accessible



segfault at ffffffff81a000e0 ip 000000000400535 sp 00007ffce4a80610 error 5 in reader

- Kernel addresses are not accessible
- Are privilege checks also done when executing instructions out of order?

• Adapted code



```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

#### • Adapted code



```
*(volatile char*)0;
array[84 * 4096] = 0; // unreachable
```

• Static code analyzer is not happy

1 warning: Dereference of null pointer
2 \*(volatile char\*)0;





• "Unreachable" code line was actually executed



• Flush+Reload over all pages of the array



- "Unreachable" code line was actually executed
- Exception was only thrown afterwards





• Combine the two things



• Combine the two things

• Then check whether any part of array is cached



• Flush+Reload over all pages of the array



• Index of cache hit reveals data



 $\bullet~\mbox{Flush+Reload}$  over all pages of the array



- Index of cache hit reveals data
- Permission check is in some cases not fast enough





×

File Edit View Search Terminal Help

mschwarz@lab86:~/Documents\$

### CAN YOU ENHANCE THAT



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# AND IN OTHER NEWS....

RELITION

# WE'RE ALL DOOMED, SANDRA.

### Not so fast...

• Kernel addresses in user space are a problem

- Kernel addresses in user space are a problem
- Why don't we take the kernel addresses...







• ...and remove them if not needed?



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- ...and remove them if not needed?
- User accessible check in hardware is not reliable



• Let's just unmap the kernel in user space



- Let's just unmap the kernel in user space
- Kernel addresses are then no longer present



- Let's just unmap the kernel in user space
- Kernel addresses are then no longer present
- Memory which is not mapped cannot be accessed at all





#### **KAISER** /'kAIZƏ/ 1. [german] Emperor, ruler of an empire 2. largest penguin, emperor penguin

Kernel Address Isolation to have Side channels Efficiently

Removed







• We published KAISER in July 2017



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- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)



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- Apple implemented it in macOS 10.13.2 and called it "Double Map"



- We published KAISER in July 2017
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it "Double Map"
- All share the same idea: switching address spaces on context switch

### Meltdown and Spectre







### **Meltdown and Spectre**





# **SPECTRE**





# **Prosciutto**



# Funghi













# **Speculative Cooking**












• Mistrains branch prediction



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- CPU speculatively executes code which should not be executed



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- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls



- Mistrains branch prediction
- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls
- $\rightarrow\,$  Spectre "convinces" program to execute code



index = 
$$0;$$





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index = 
$$1;$$









index = 
$$2;$$









index = 
$$3;$$



## Spectre (variant 1)





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index = 
$$4;$$











index = 
$$5;$$



Spectre (variant 1)







index = 
$$6;$$



Spectre (variant 1)



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## Animal\* a = bird;
































• Trivial approach: disable speculative execution



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- No wrong speculation if there is no speculation



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- Problem: massive performance hit!



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- Also: How to disable it?



- Trivial approach: disable speculative execution
- No wrong speculation if there is no speculation
- Problem: massive performance hit!
- Also: How to disable it?
- Speculative execution is deeply integrated into CPU





• Workaround: insert instructions stopping speculation



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- $\rightarrow\,$  insert after every bounds check





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  - ×86: LFENCE, ARM: CSDB





- Workaround: insert instructions stopping speculation
- $\rightarrow\,$  insert after every bounds check
  - ×86: LFENCE, ARM: CSDB
  - Available on all Intel CPUs, retrofitted to existing ARMv7 and ARMv8





• Speculation barrier requires compiler supported



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- Already implemented in GCC, LLVM, and MSVC



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- Can be automated (MSVC)  $\rightarrow$  not really reliable



- Speculation barrier requires compiler supported
- Already implemented in GCC, LLVM, and MSVC
- Can be automated (MSVC)  $\rightarrow$  not really reliable
- Explicit use by programmer: \_\_builtin\_load\_no\_speculate

```
// Unarstected
und an rev[3]:
unt get_value(unsigned int m) {
  int the:
  if in x 31 {
    tmp = array[n]
  } else {
  ï
 return tho:
```

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- Programmer has to fully understand vulnerability





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- Speculation barrier works if affected code constructs are known
- Programmer has to fully understand vulnerability
- Automatic detection is not reliable
- Non-negligible performance overhead of barriers

• Indirect Branch Restricted Speculation (IBRS):

୦-I-୦-I-୦ I-୦-I-୦-I ୦-I-୦-I-୦ I-୦-I-୦-I

- Indirect Branch Restricted Speculation (IBRS):
  - Do not speculate based on anything before entering IBRS mode

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- Indirect Branch Predictor Barrier (IBPB):

0-1-0-1-0 1-0-1-0-1 0-1-0-1-0 1-0-1-0-1

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- Single Thread Indirect Branch Predictors (STIBP):

Indirect Branch
 Do not spec
 → lesser privile

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Intel released microcode updates

- Indirect Branch Restricted Speculation (IBRS):
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  - $\rightarrow\,$  lesser privileged code cannot influence predictions
- Indirect Branch Predictor Barrier (IBPB):
  - Flush branch-target buffer
- Single Thread Indirect Branch Predictors (STIBP):
  - Isolates branch prediction state between two hyperthreads

୦-I-୦-I-୦ I-୦-I-୦-I ୦-I-୦-I-୦ I-୦-I-୦-I Retpoline (compiler extension)





```
push <call_target>
call 1f
2: ; speculation will continue here
lfence ; speculation barrier
jmp 2b ; endless loop
1:
lea 8(%rsp), %rsp ; restore stack pointer
ret ; the actual call to <call_target>
```

 $\rightarrow\,$  always predict to enter an endless loop

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- instead of the correct (or wrong) target function  $\rightarrow$  performance?
- On Broadwell or newer:
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  - $\rightarrow$  microcode patches to prevent that





• ARM provides hardened Linux kernel

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- Clears branch-predictor state on context switch



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- Either via instruction (BPIALL)...



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- ...or workaround (disable/enable MMU)



- ARM provides hardened Linux kernel
- Clears branch-predictor state on context switch
- Either via instruction (BPIALL)...
- ...or workaround (disable/enable MMU)
- Non-negligible performance overhead ( $\approx$  200-300 ns)

• Prevent access to high-resolution timer



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- $\rightarrow~\mbox{Own}$  timer using timing thread





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- Prevent access to high-resolution timer
- $\rightarrow~{\rm Own}$  timer using timing thread
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- $\rightarrow\,$  Cache eviction through memory accesses
- Just move secrets into secure world
- $\rightarrow\,$  Spectre works on secure enclaves



• Out-of-Order Execution

#### Spectre

• Speculative Execution (subset of Out-of-Order Execution)

- Out-of-Order Execution
- has nothing to do with branch prediction

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### Spectre

• performs only legal memory accesses

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  - exception handling

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 $\rightarrow$  two papers, two names, etc.

# What if we want to modify data?





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- Cells leak  $\rightarrow$  repetitive refresh necessary
- Maximum interval between refreshes to guarantee data integrity
- Cells leak faster upon proximate accesses  $\rightarrow$  Rowhammer



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• There are two different hammering techniques

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- #1: Hammer one row next to victim row and other random rows

- There are two different hammering techniques
- #1: Hammer one row next to victim row and other random rows
- #2: Hammer two rows neighboring victim row

- There are three different hammering techniques
- #1: Hammer one row next to victim row and other random rows
- #2: Hammer two rows neighboring victim row
- #3: Hammer only one row next to victim row



























## DRAM bank \_ -111111111111111 1111111111111111 1111111111111111 1111111111111111 111111111111111 111111111111111 111111111111111 1111111111111111

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## DRAM bank \_ -111111111111111 1111111111111111 1111111111111111 1111111111111111 111111111111111 111111111111111 111111111111111 1111111111111111

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- $\bullet~$  They are not random  $\rightarrow~$  highly reproducible flip pattern!
  - 1. Choose a (kernel) data structure that you can place at arbitrary memory locations
  - 2. Scan for "good" flips
  - 3. Place (kernel) data structure there
  - 4. Trigger bit flip again

• Many applications perform actions as root

- Many applications perform actions as root
- They can be used by unprivileged users as well

- Many applications perform actions as root
- They can be used by unprivileged users as well
- sudo




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- $\rightarrow\,$  use ECC memory to mitigate bit flips



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  - what if the "too aggressive" changes over time?
  - what if attackers come up with slightly better attacks?



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  - too cautious? waste of energy
  - what if the "too aggressive" changes over time?
  - what if attackers come up with slightly better attacks?
  - $\rightarrow$  difficult to optimize with an intelligent adversary





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- $\rightarrow\,$  for years we solely optimized for performance



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• the side channels were documented in the Intel manual



After learning about a side channel you realize:

- the side channels were documented in the Intel manual
- only now we understand the implications



Motor Vehicle Deaths in U.S. by Year

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## A unique chance to

• rethink processor design



#### A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)



#### A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)
- dedicate more time into identifying problems and not solely in mitigating known problems



# Microarchitectural Attacks: Meltdown and Spectre

#### **Daniel Gruss**

April 21, 2018

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