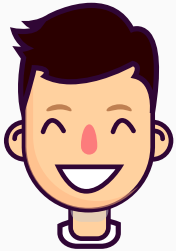
Hardware-Software Co-Design to Eliminate Cache Leakage

Lukas Giner, Daniel Gruss

June 11, 2019

Graz University of Technology

Who am I?



Lukas Giner

PhD student @ Graz University of Technology

@redrabbyte

lukas.giner@iaik.tugraz.at

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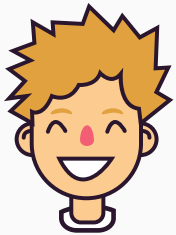


Daniel Gruss

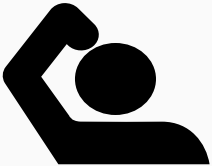
Asst. Prof. @ Graz University of Technology

@lavados

daniel.gruss@iaik.tugraz.at

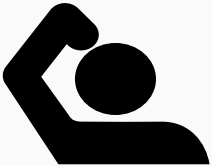

side channel
= obtaining meta-data and
deriving secrets from it
CHANGE MY MIND

Side Channel or not?



Side Channel or not?

- Profiling cache utilization with performance counters?



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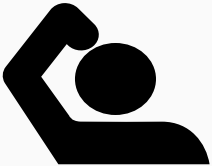

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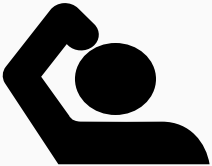

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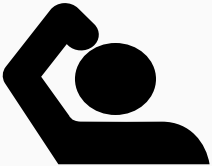

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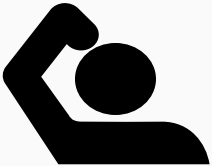

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Speculative Side-Channel Attacks?

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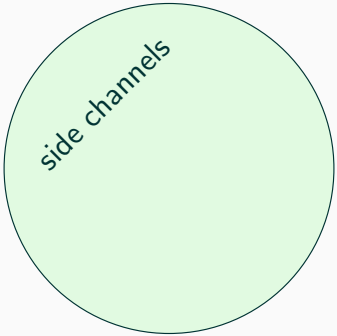

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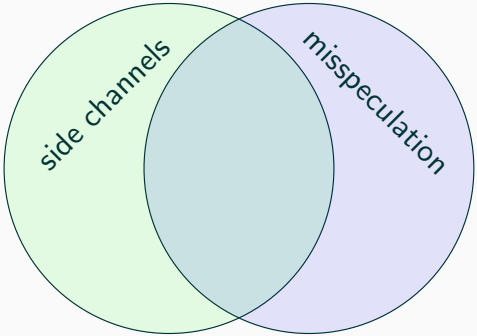

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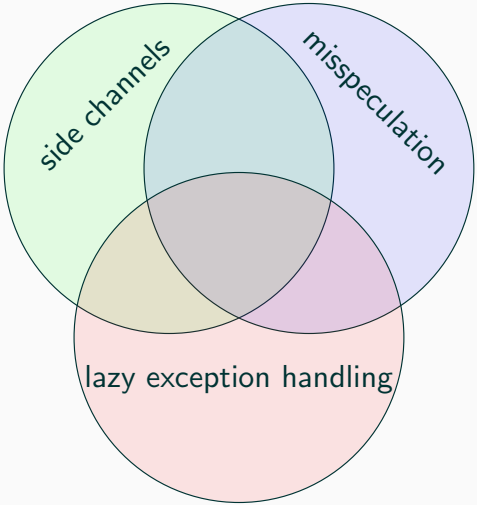

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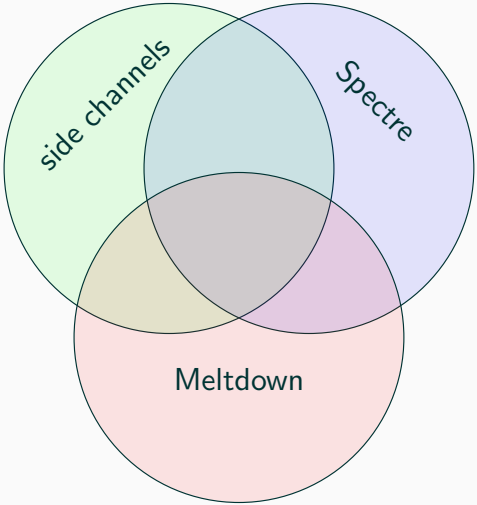

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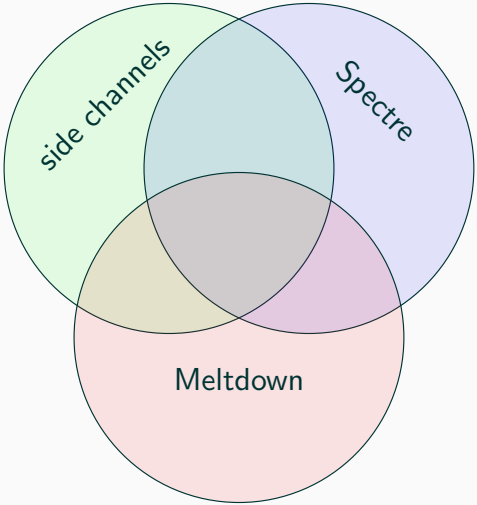

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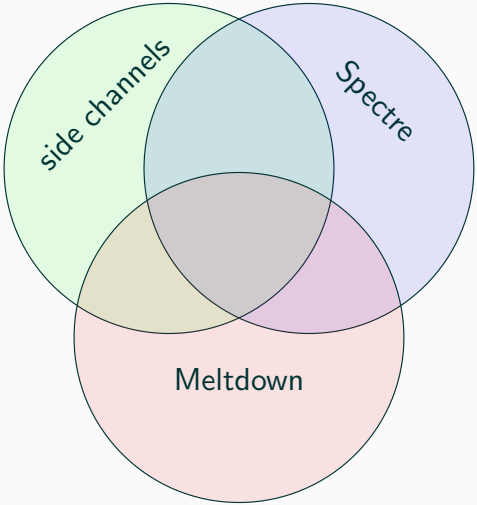

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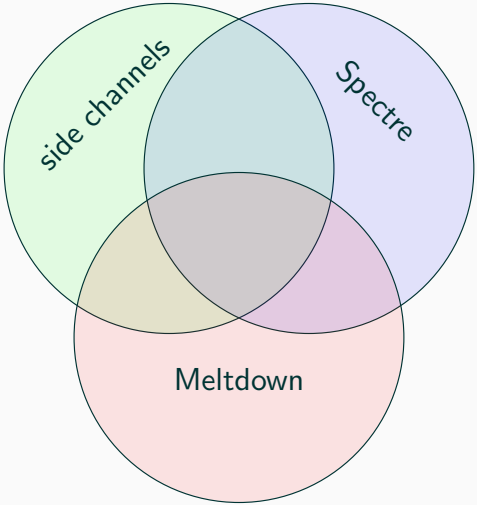

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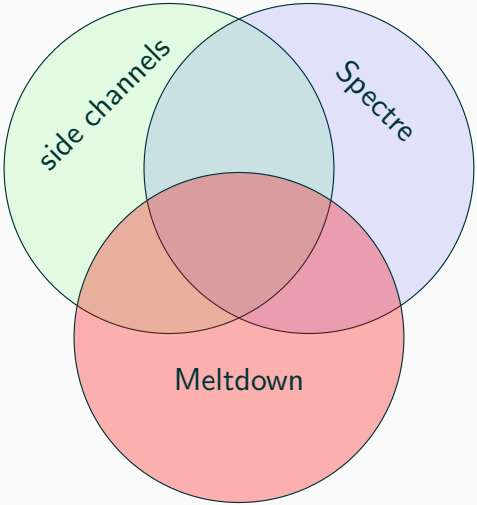
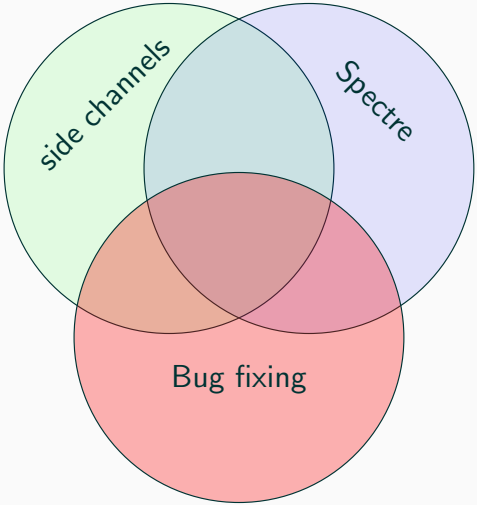
- Let's be more precise
- $\rightarrow$ then we can think about actual mitigations

Speculative Side-Channel Attacks?



Speculative Side-Channel Attacks?



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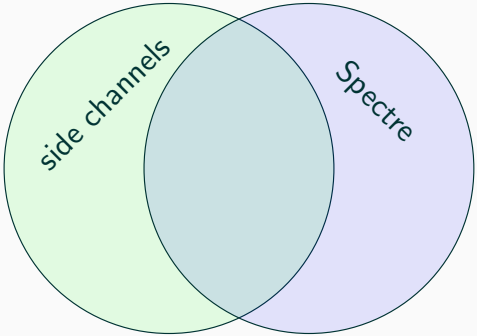

But what about these two?

- CPU Caches are a shared resource

The Problem with Cache Side Channels

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  $\rightarrow$ there's probably a side-channel

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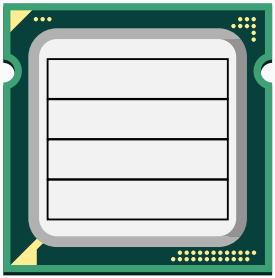
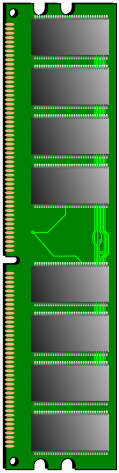
How do caches work?

```
printf("%d", i);
printf("%d", i);
```





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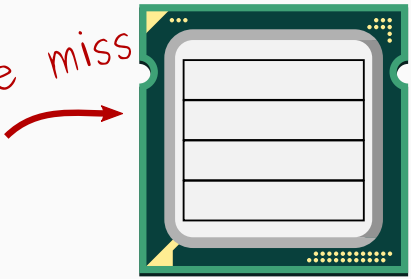

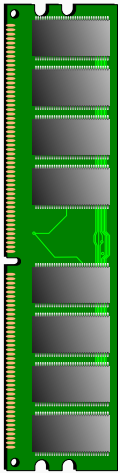

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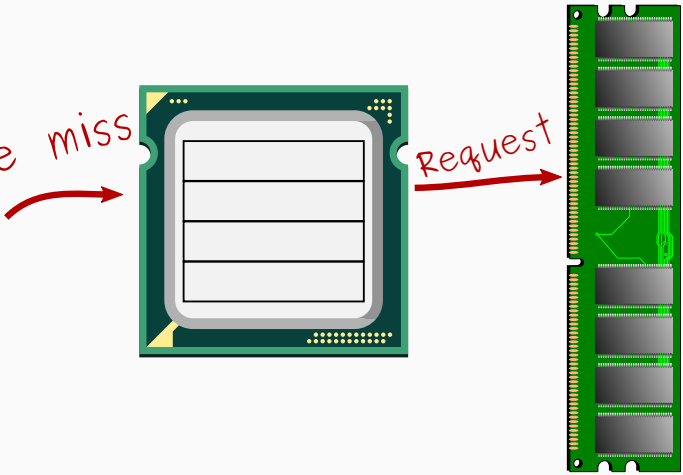

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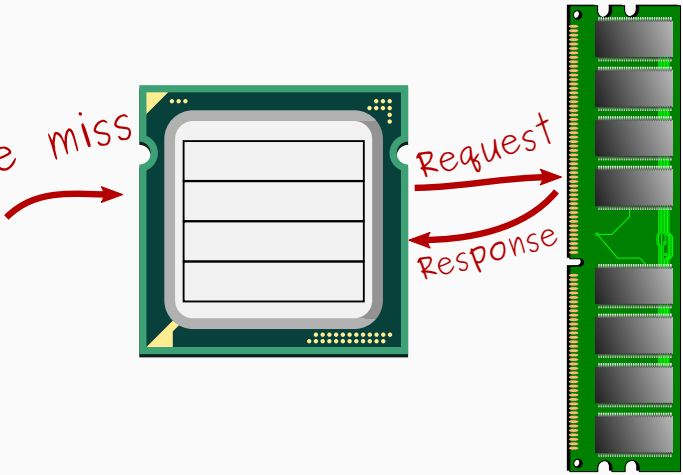

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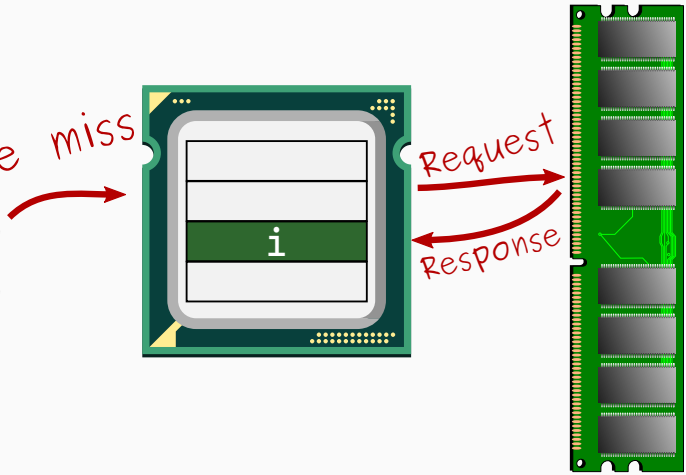

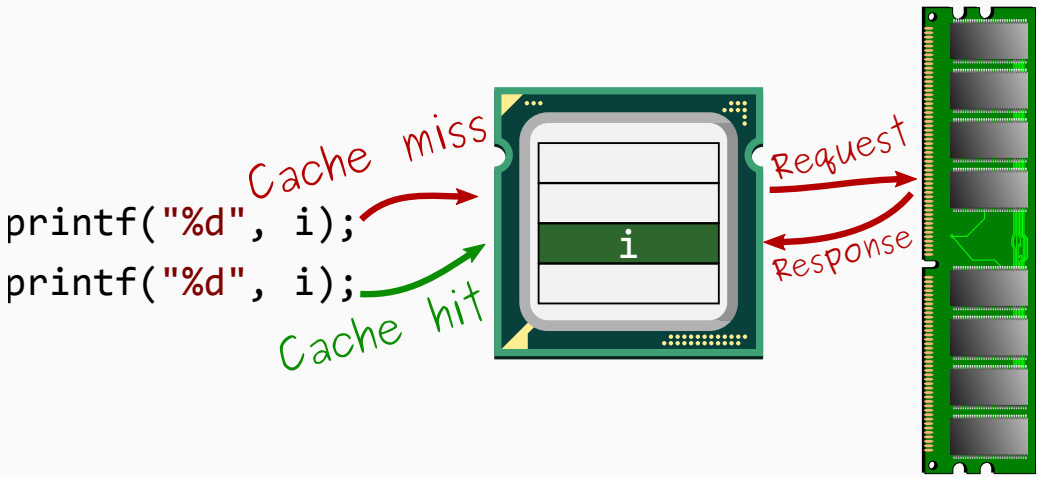
printf("%d", i);
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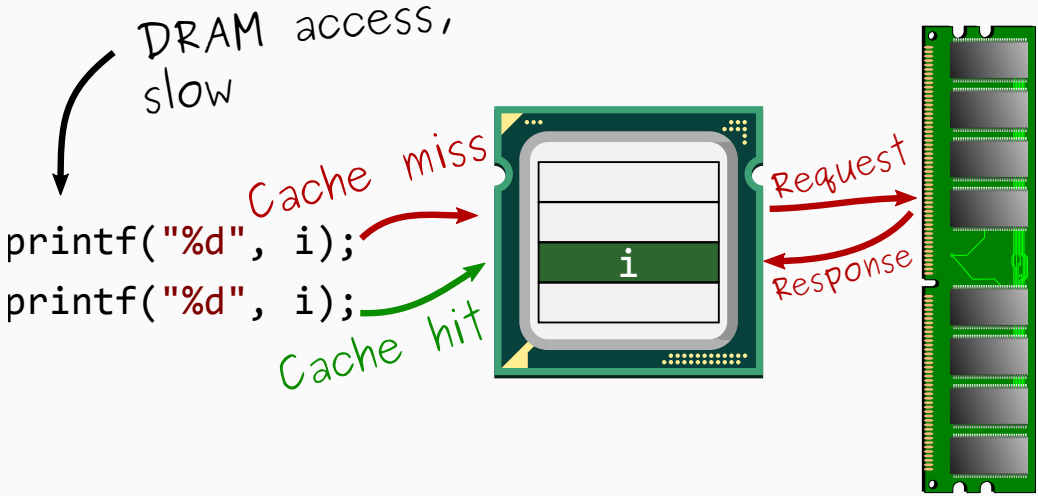
Cache miss
Cache hit
i
Request
Response


DRAM access, slow
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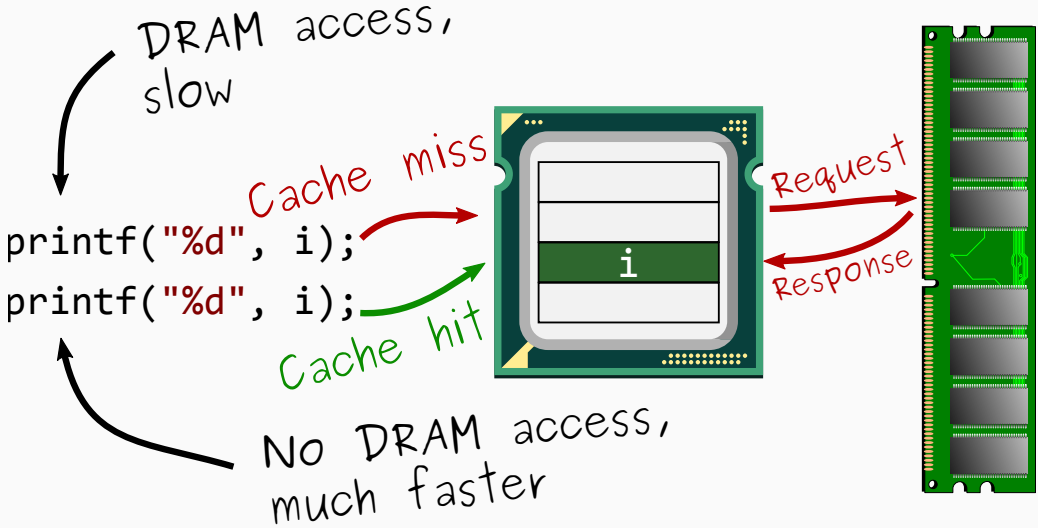
DRAM access, slow
printf("%d", i);
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Cache hit
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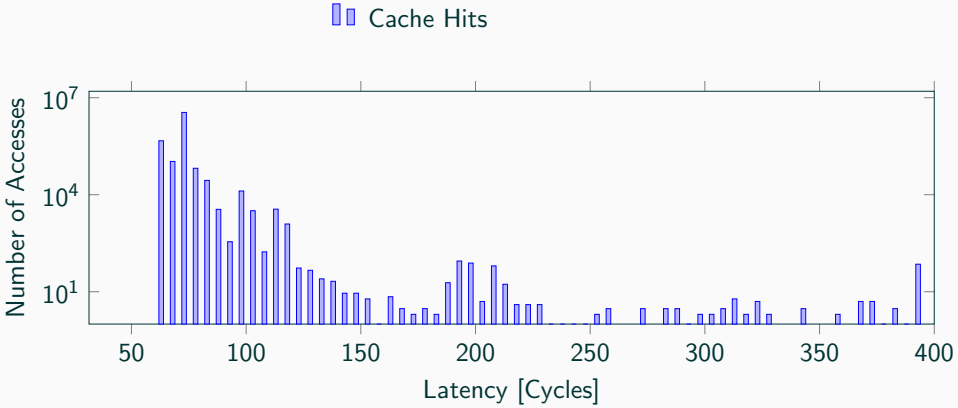
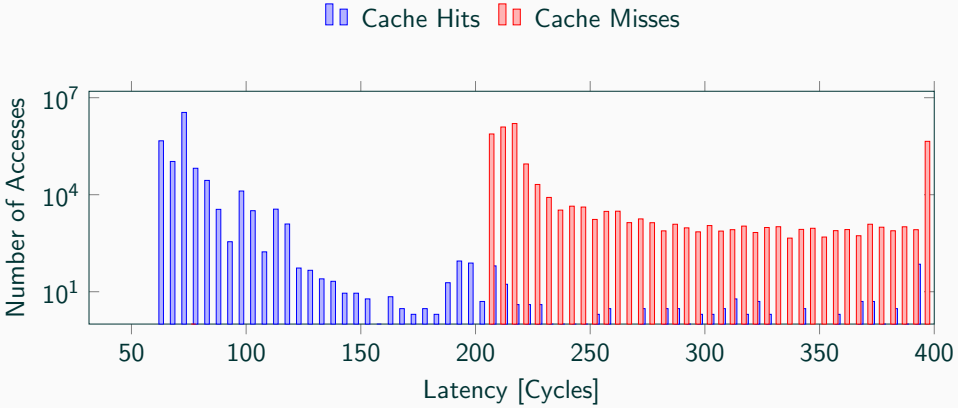
Request
Response
No DRAM access, much faster


Cache Hits
Number of Accesses
10^7
10^4
10^1
50
100
150
200
250
300
350
400
Latency [Cycles]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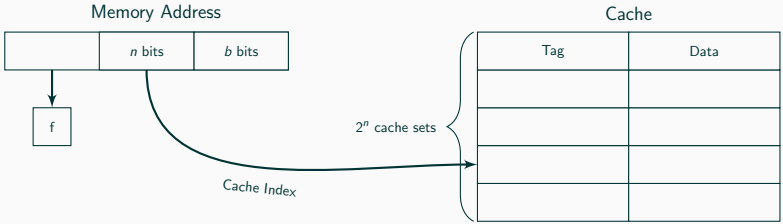
2-way set associativity



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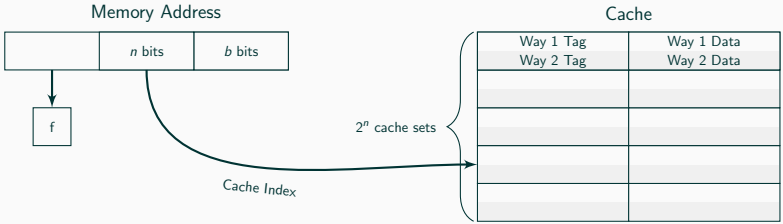

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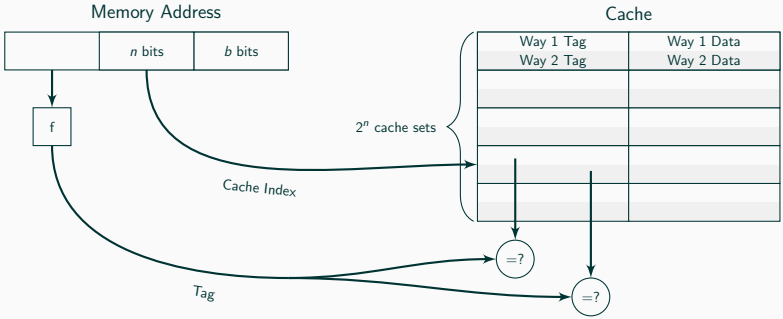

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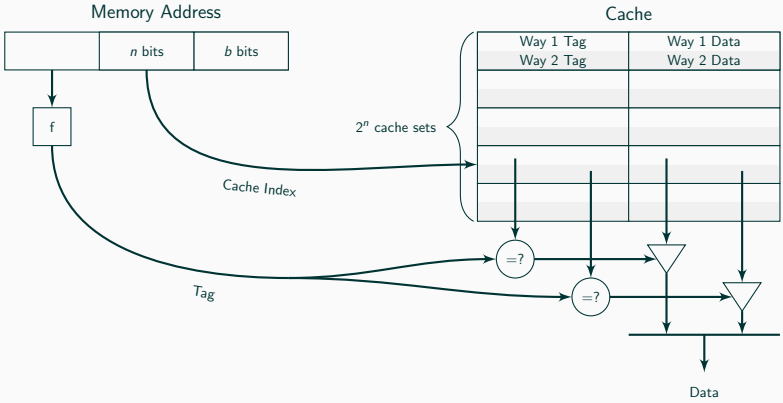

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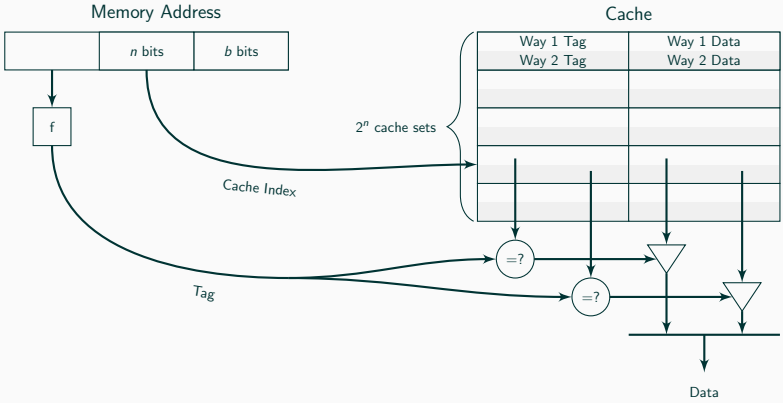
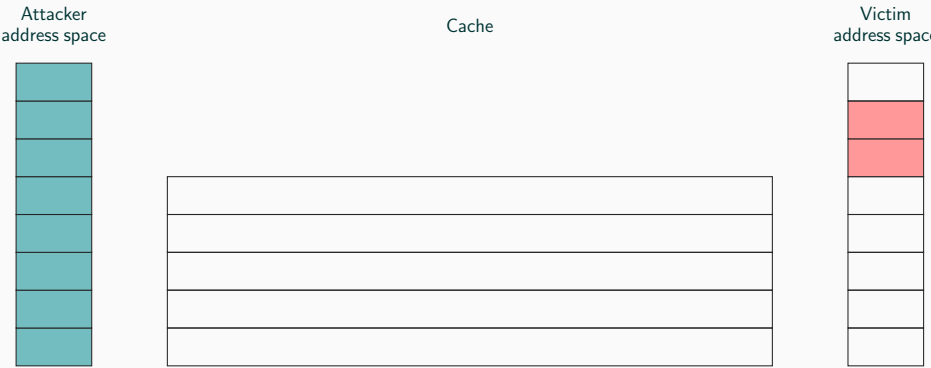
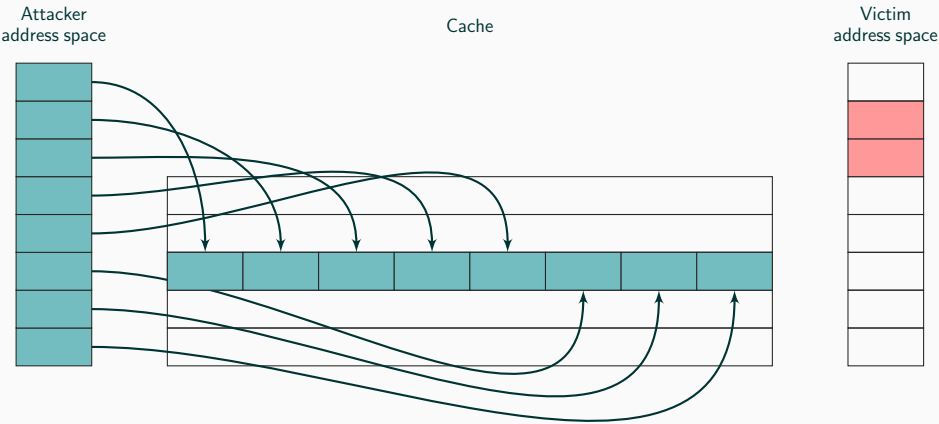


→ replacement policy


Attacker
address space
Cache
Victim
address space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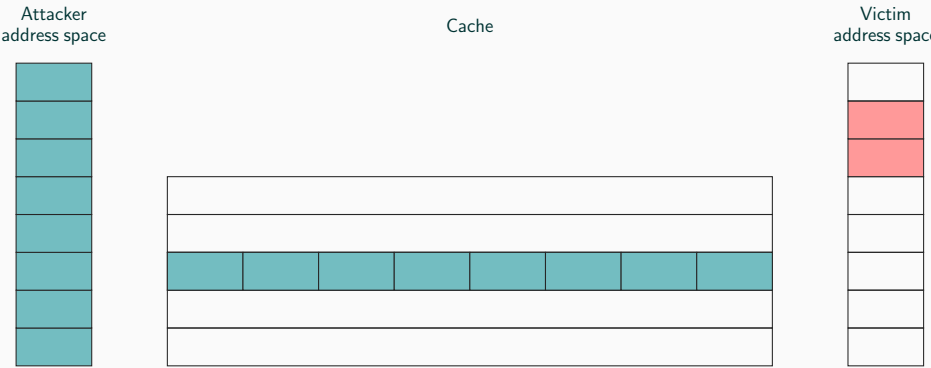
Attacker
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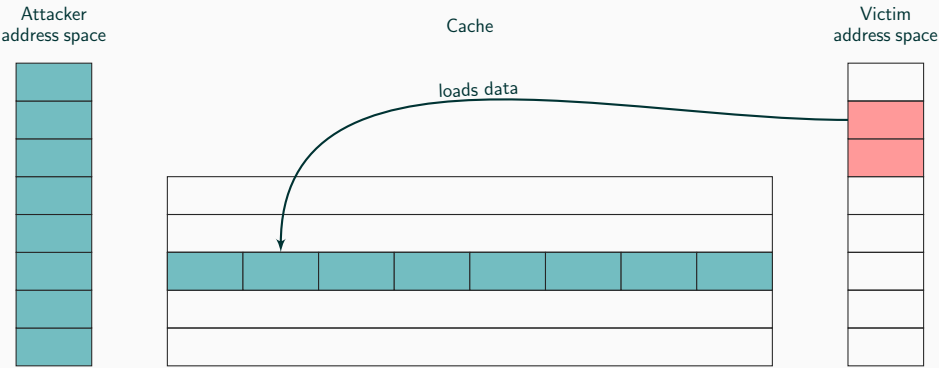
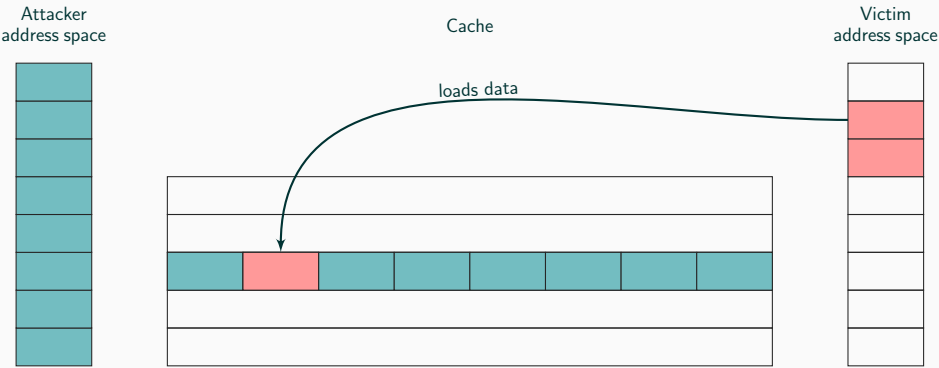
Cache
Victim
address space


Attacker
address space
Cache
Victim
address space
loads data


Attacker
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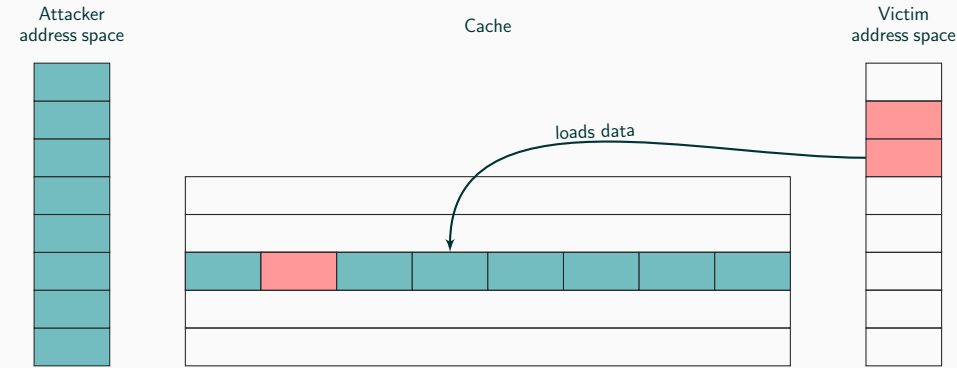
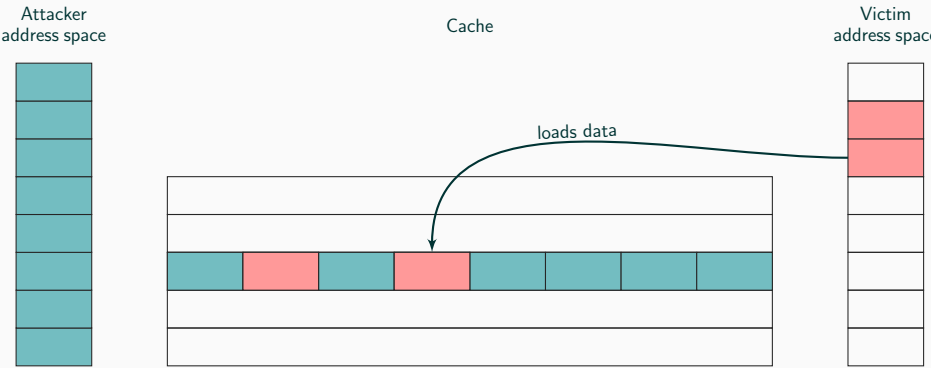
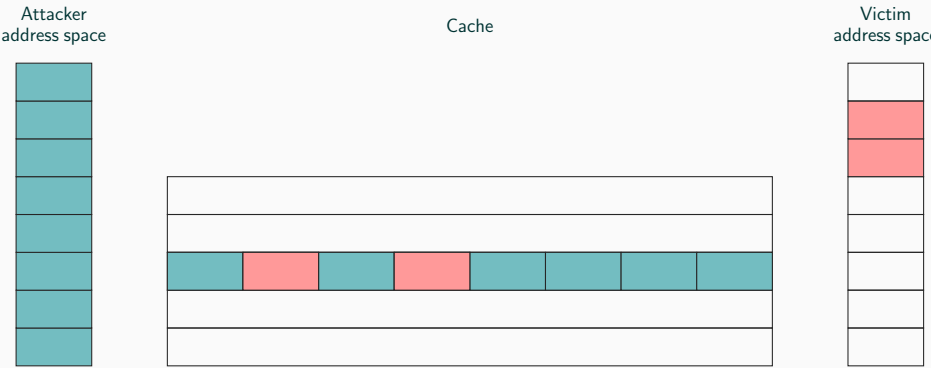
Cache
Victim
address space
loads data


Attacker
address space
Cache
Victim
address space
loads data


Attacker
address space
Cache
Victim
address space
loads data


Attacker
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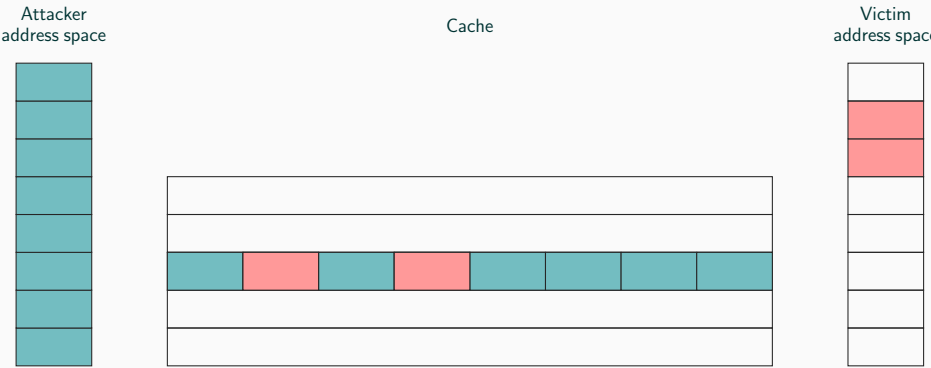
Attacker
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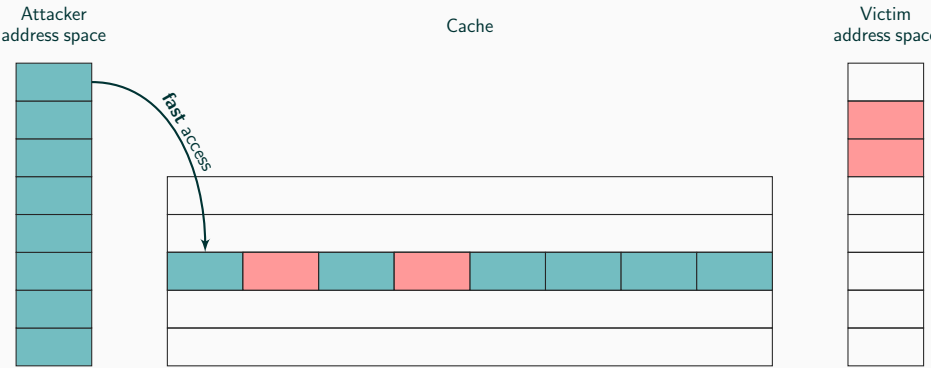
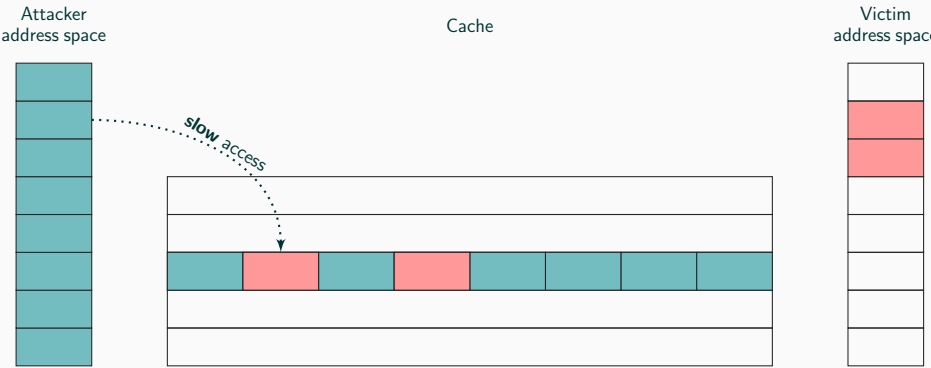
Cache
Victim
address space


Attacker
address space
Cache
Victim
address space
fast access


Attacker
address space
Cache
Victim
address space
slow access

ScatterCache

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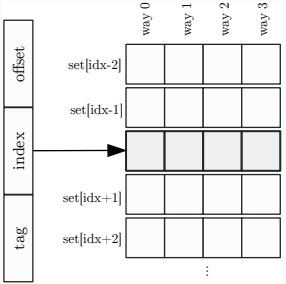

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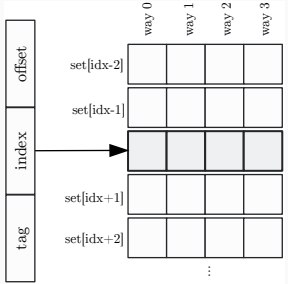
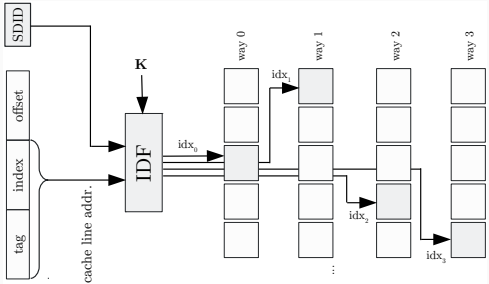
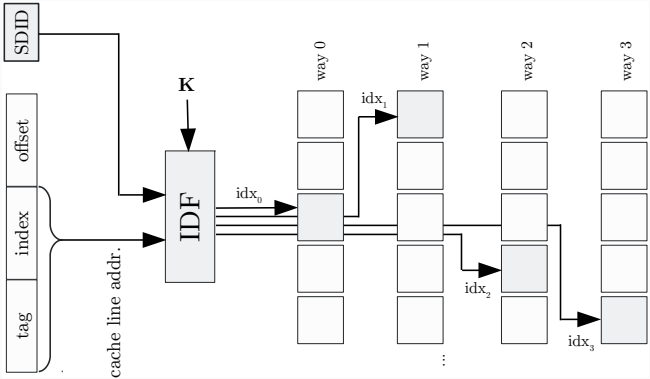
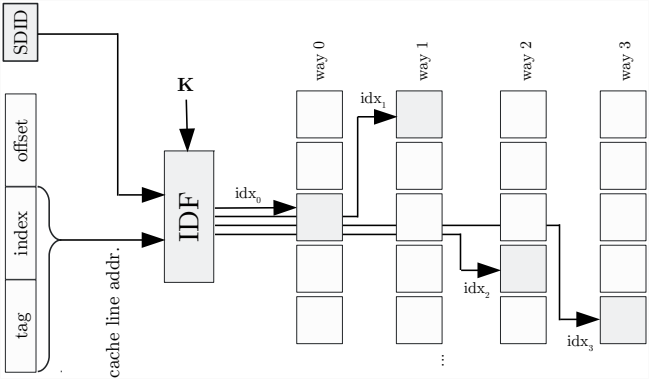


let's do this:





- Index Derivation Function (IDF) takes an address and returns a cache set



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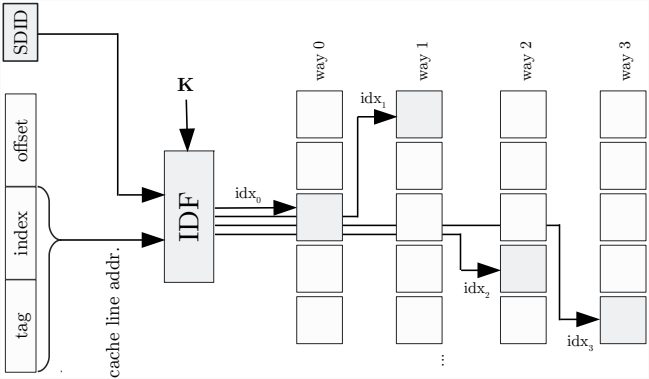
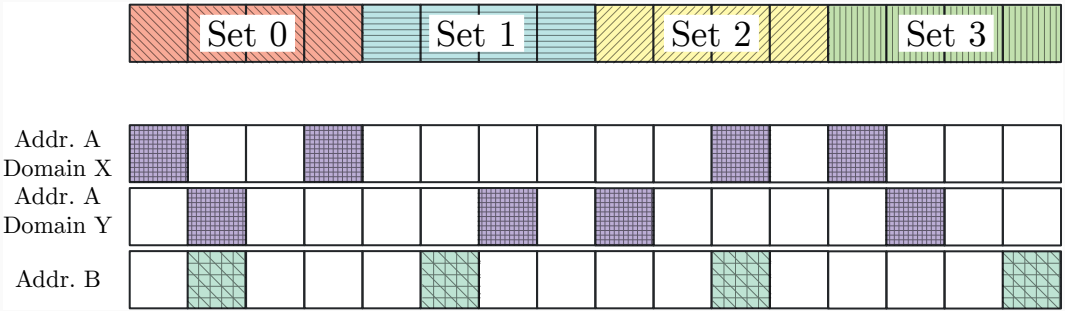
- Depends on hardware key K and optional Security Domain ID (SDID)



- Index Derivation Function (IDF) takes an address and returns a cache set
- Depends on hardware key K and optional Security Domain ID (SDID)
- → unique combination of cache lines for each address


Set 0
Set 1
Set 2
Set 3
Addr. A
Domain X
Addr. A
Domain Y
Addr. B

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- Evicting an address with 99% certainty needs 275 addresses for 8-way cache, instead of ≈ 8 for standard Prime+Probe
- Constructing this set requires $\approx 2^{25}$ profiled victim accesses, compared to less than 100 accesses for standard, noise-free Prime+Probe

- Micro benchmarks GAP, MiBench, Imbench, scimark2 on gem5 full system simulator

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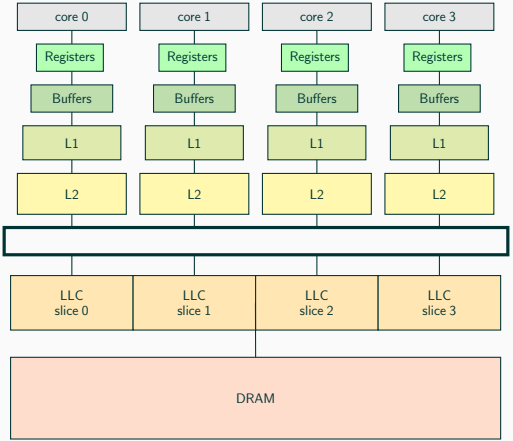
- Cache hit rate always at or above levels of set-associative cache with random replacement
- Typically $2\% - 4\%$ below LRU on micro benchmarks, $0\% - 2\%$ for SPEC

ConTExT

Where can data be?



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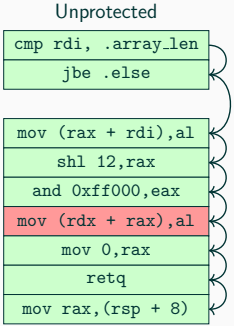
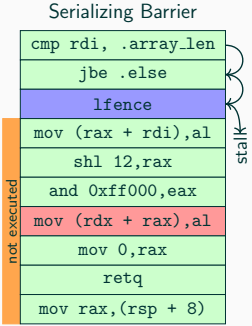
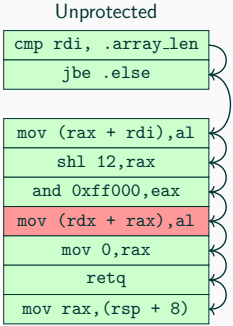
  - Pages
  - Cache Lines (in caches and buffers)
  - Registers

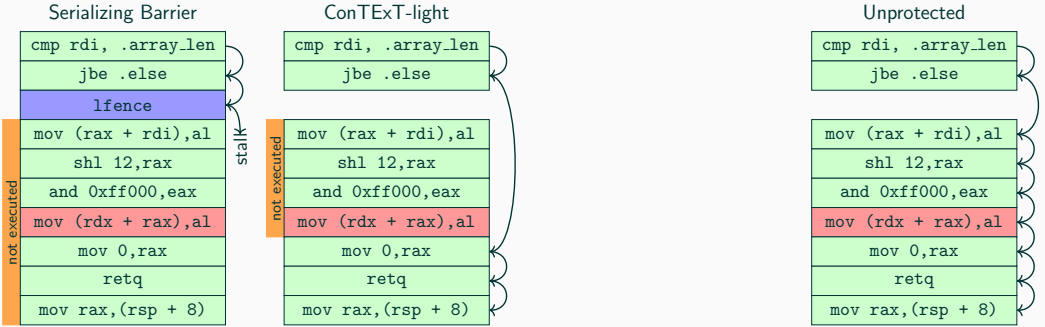

Unprotected
cmp rdi, .array_len
jbe .else
mov (rax + rdi),al
shl 12,rax
and 0xff000,eax
mov (rdx + rax),al
mov 0,rax
retq
mov rax,(rsp + 8)

ConTExT Comparison





ConTExT Comparison



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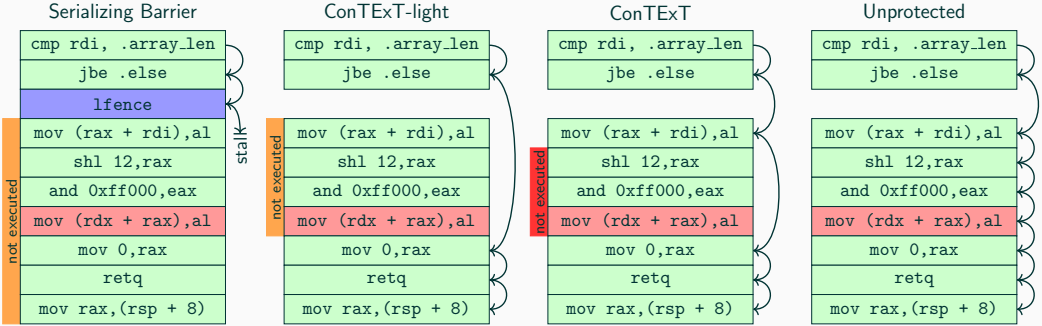

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- Split stack into protected and unprotected half
- Stack spills of unprotected data $\rightarrow$ stay unprotected as long as they stay in the cache

Papers co-funded by Intel SCAP

C. Canella, J. Van Bulck, M. Schwarz, M. Lipp, B. von Berg, P. Ortner, F. Piessens, D. Evtyushkin, and D. Gruss. A Systematic Evaluation of Transient Execution Attacks and Defenses. In: USENIX Security Symposium. 2019.

D. Gruss, E. Kraft, T. Tiwari, M. Schwarz, A. Trachtenberg, J. Hennessey, A. Ionescu, and A. Fogh. Page Cache Attacks. In: CCS. 2019.

M. Schwarz, C. Canella, L. Giner, and D. Gruss. Store-to-Leak Forwarding: Leaking Data on Meltdown-resistant CPUs. In: arXiv:1905.05725 (2019).

M. Schwarz, M. Lipp, D. Moghimi, J. Van Bulck, J. Stecklina, T. Prescher, and D. Gruss. ZombieLoad: Cross-Privilege-Boundary Data Sampling. In: arXiv:1905.05726 (2019).

M. Schwarz, R. Schilling, F. Kargl, M. Lipp, C. Canella, and D. Gruss. ConTExT: Leakage-Free Transient Execution. In: arXiv:1905.09100 (2019).

M. Schwarz, S. Weiser, and D. Gruss. Practical Enclave Malware with Intel SGX. In: DIMVA. 2019.

M. Werner, T. Unterluggauer, L. Giner, M. Schwarz, D. Gruss, and S. Mangard. ScatterCache: Thwarting Cache Attacks via Cache Set Randomization. In: USENIX Security Symposium. 2019.

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- many attacks out there

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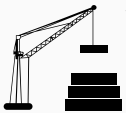
- important to distinguish between different attacks

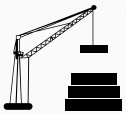
Hardware-Software Co-Design to Eliminate Cache Leakage

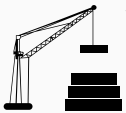
Lukas Giner, Daniel Gruss

June 11, 2019

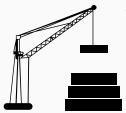
Graz University of Technology







- Compiler Extension



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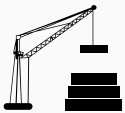

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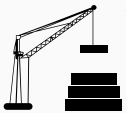

- Compiler Extension
- Linux Patch
- CPU Emulation in Bochs
- Native via uncacheable memory (ConTExT-light)

Benchmark	SPEC Score		Overhead
	Baseline	ConTExT	[%]
600.perlbench_s	7.03	6.86	+2.42
602.gcc_s	11.90	11.80	+0.84
605.mcf_s	9.06	9.16	−1.10
620.omnetpp_s	5.07	4.81	+5.13
623.xalancbmk_s	6.06	5.95	+1.82
625.x264_s	9.25	9.25	0.00
631.deepsjeng_s	5.26	5.22	+0.76
641.leela_s	4.71	4.64	+1.48
648.exchange2_s	*would require Fortran runtime*		
657.xz_s	12.10	12.10	0.00
Average			+1.26

Table 1: Performance of the ConTExT split stack using the SPECspeed 2017 integer benchmark.