Software-based Microarchitectural Attacks

Daniel Gruss

April 19, 2018

Graz University of Technology

Whoami

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Timeline of Meltdown and Spectre

- Both vulnerabilities existed for many years

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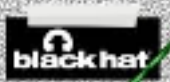
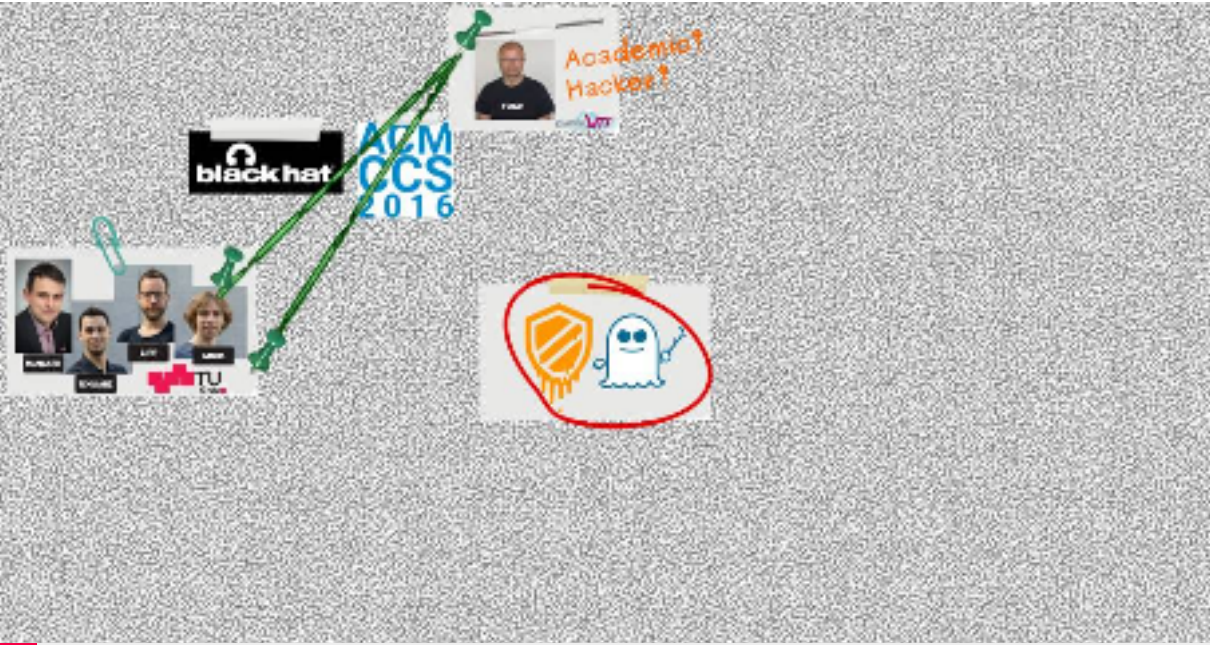
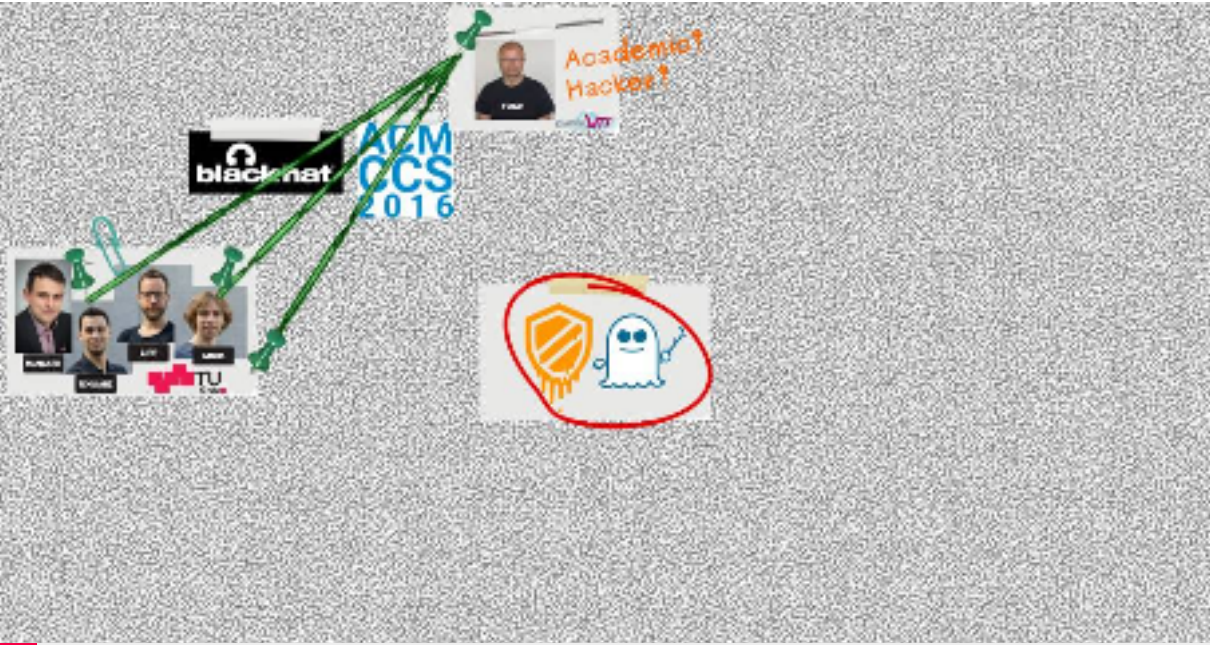
- Suddenly, 4 independent teams discover it within 6 months
- Let's create an evidence board

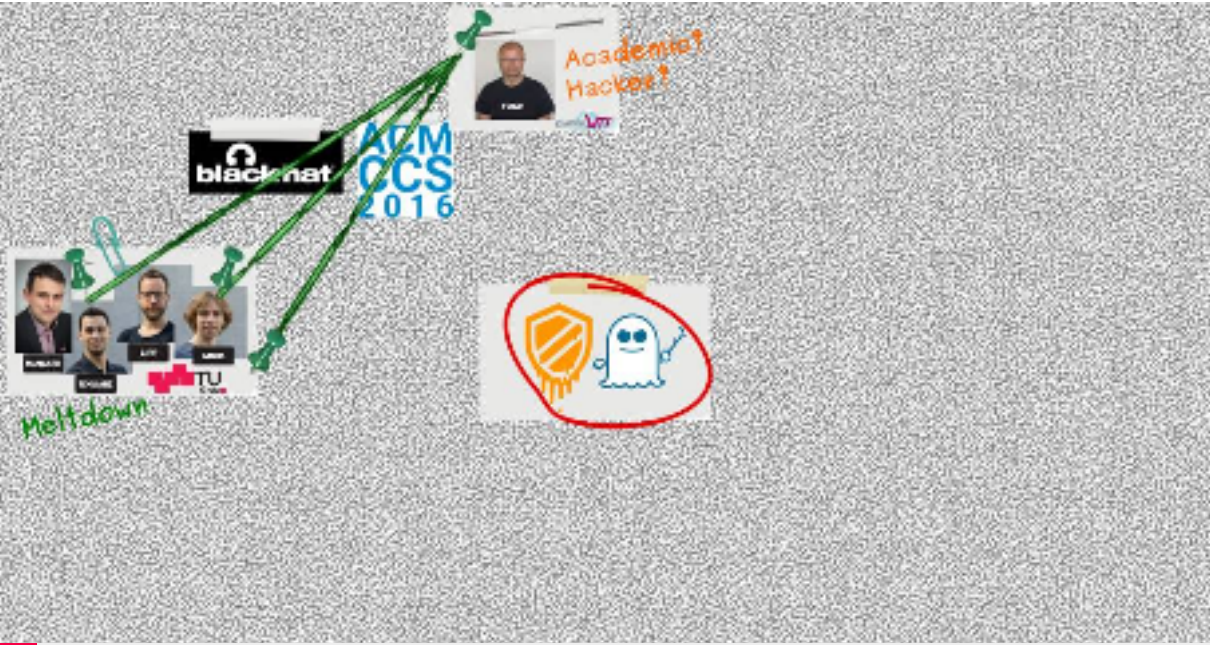

Academic?
Hacker?

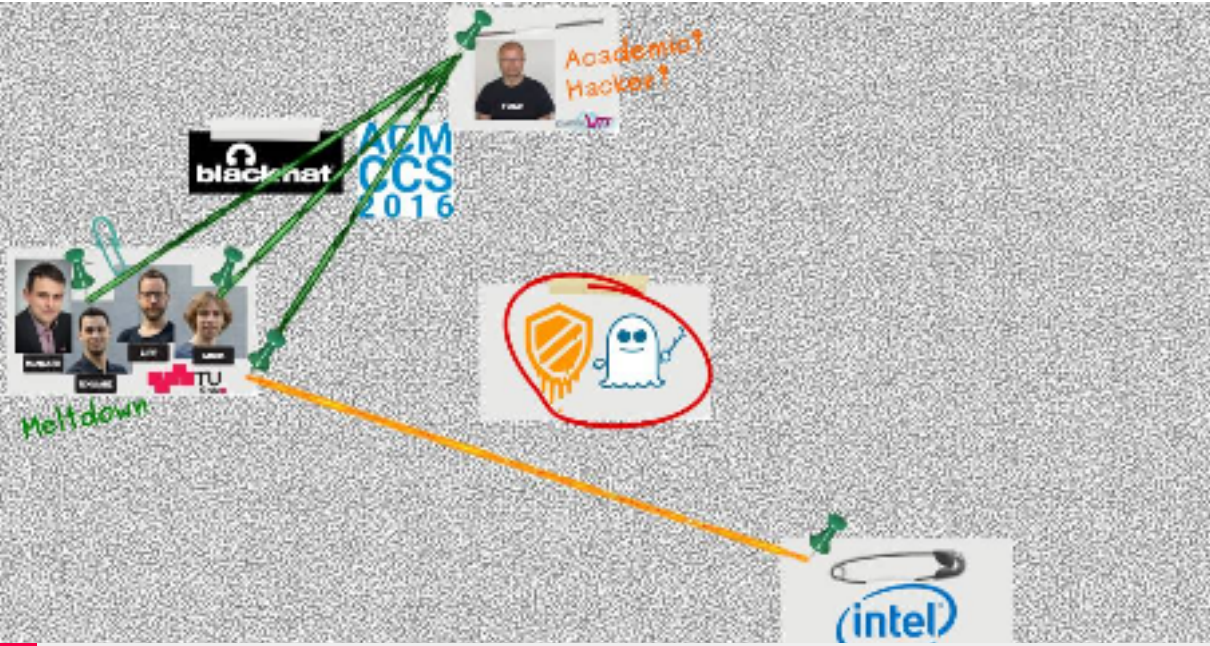

Academic?
Hacker?

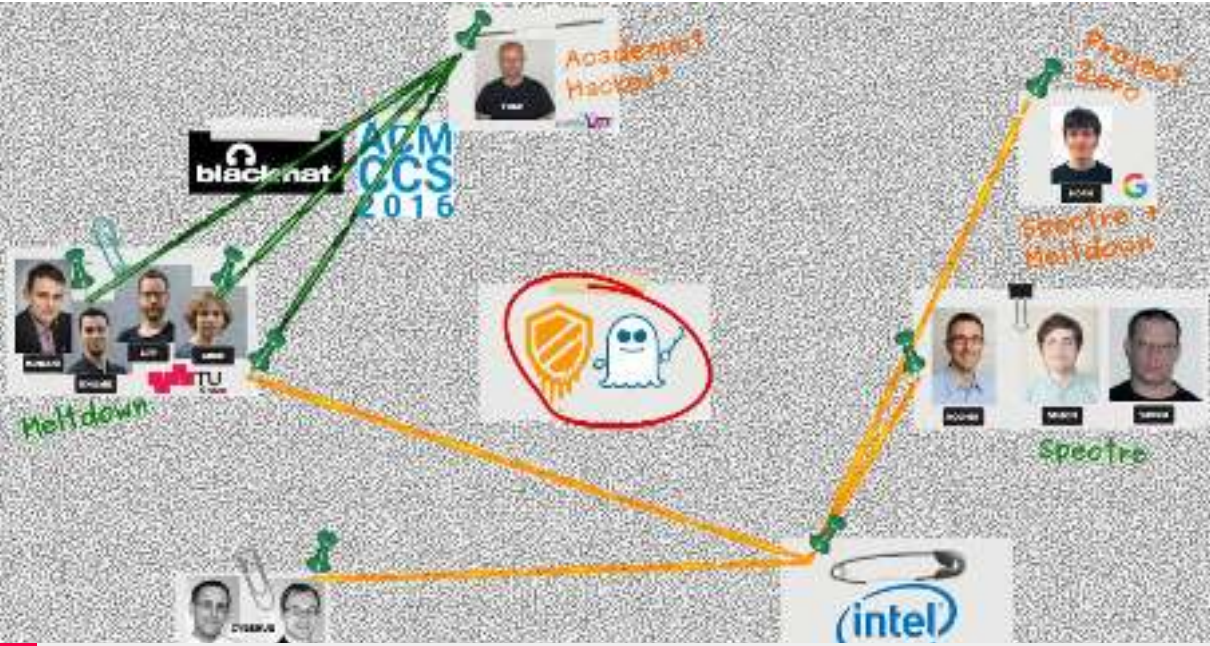

black hat

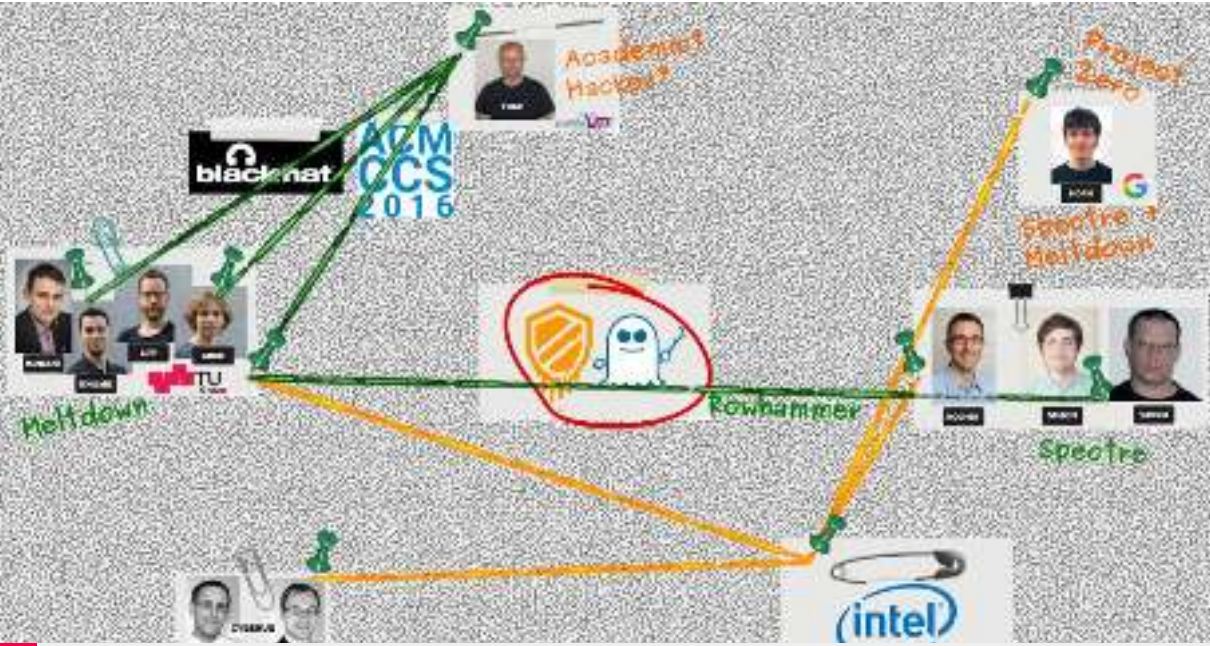

Academic?
Hacker?
black hat
ACM
CCS
2016
TU

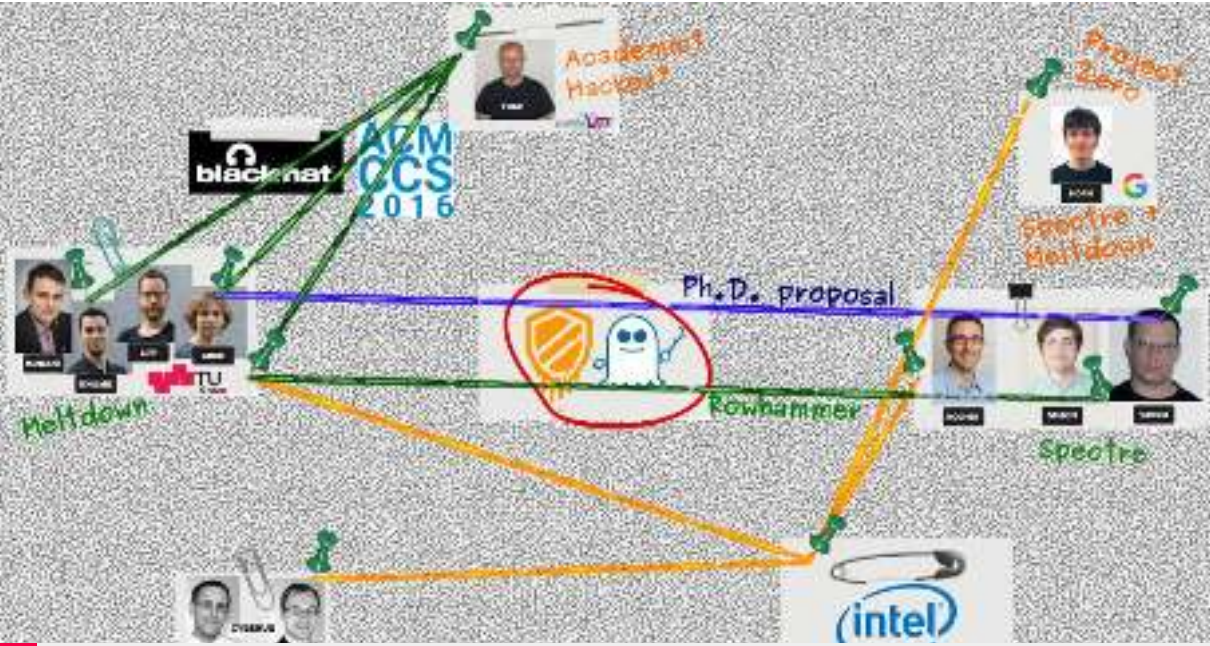

Academic?
Hacker?
black hat
ACM
CCS
2016
TU


Academic?
Hacker?
black hat
ACM
CCS
2016
TU
Meltdown


Academia?
Hacker?
black hat
ACM
CCS
2016
TU
Meltdown
intel


Academic Hacker
black hat
ACM CCS 2016
Project Zero
Spectre + Meltdown
Meltdown
Spectre
intel


Academic Hackers
Project Zero
black hat
ACM CCS 2016
Spectre + Meltdown
Meltdown
Rowhammer
Spectre
intel


Academic Hacker
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ACM CCS 2016
Spectre + Meltdown
Ph.D. proposal
TU
Meltdown
Rowhammer
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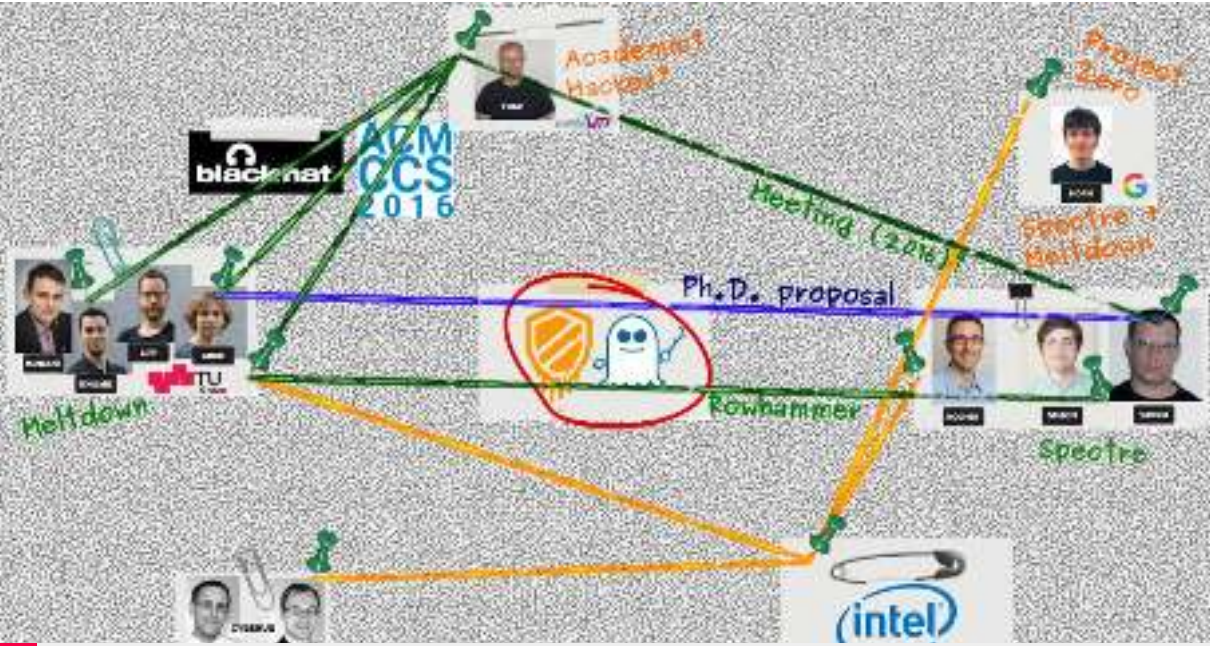
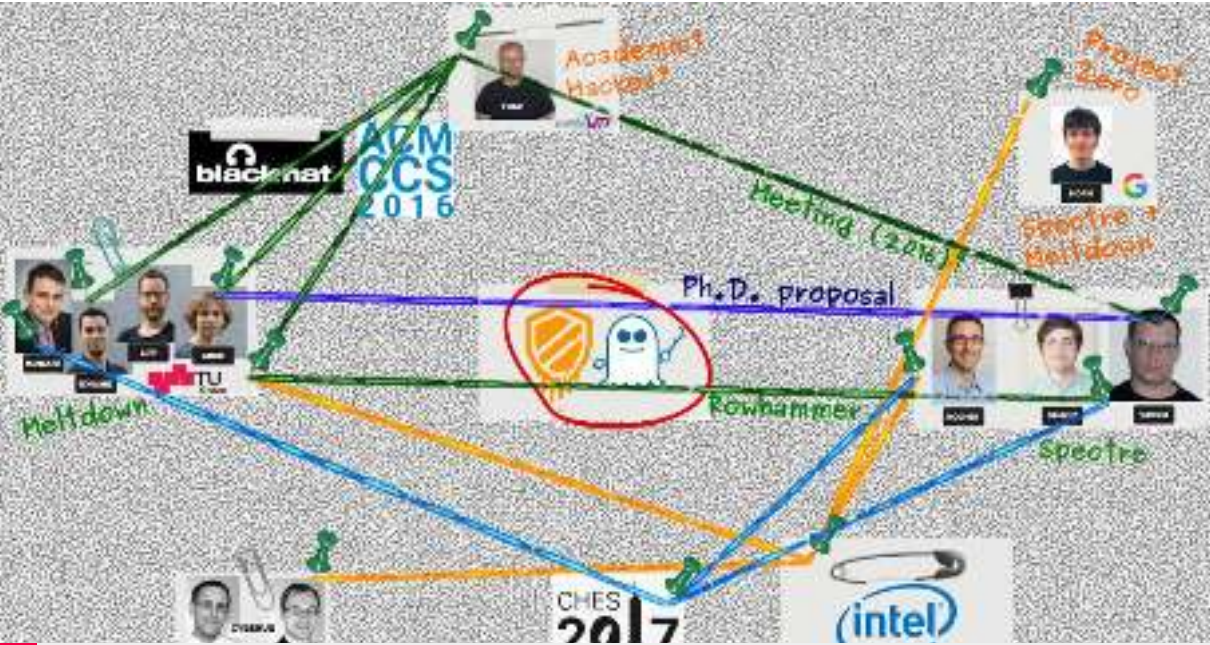
intel


Academic Hacker
Project Zero
black hat
ACM CCS 2016
Meeting (2016)
Spectre + Meltdown
Ph.D. proposal
TU
Meltdown
Rowhammer
Spectre
intel


Academic hacker
black hat
ACM CCS 2016
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Spectre + Meltdown
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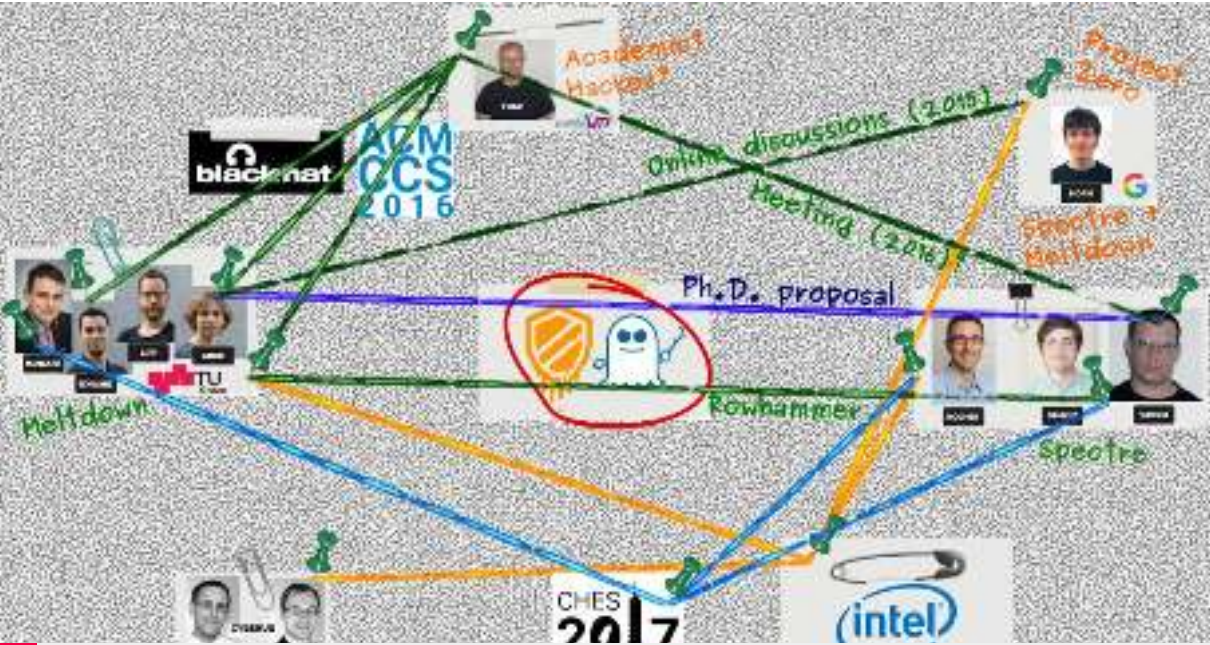
Meltdown
Rowhammer
Spectre
CHES 2017
intel


Academic hacker
Project Zero
black hat
ACM CCS 2016
online discussions (2015)
meeting (2016)
Spectre + Meltdown
Ph.D. proposal
TU
Meltdown
Rowhammer
Spectre
CHES 2017
intel

Why two names, two papers, etc?

- Two different problems

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- They only have a very loose connection

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- Two different problems
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- Two different teams had already quite matured drafts ready when learning of each other

Why two names, two papers, etc?

- Two different problems
- They only have a very loose connection
- Two different teams had already quite matured drafts ready when learning of each other
- Initially we tried to merge, but all co-authors quickly agreed that it would mix things that don't belong together

$\rightarrow$ More on that after we understand the attacks

The Fallout

You realize it is something big when...

The Fallout

You realize it is something big when...

- it is in the news, all over the world


FOX
BUSINESS
WASHINGTON, D.C.
WASHINGTON, D.C.
WINTER STORM
NEWS
› ALERT
INTEL REVEALS DESIGN FLAW THAT
COULD ALLOW HACKERS TO ACCESS DATA
FOX
BUSINESS
NETWORK
@FOXBUSINESS


DEVELOPING STORY
COMPUTER CHIP FLAWS IMPACT BILLIONS OF DEVICES
LIVE
CNN
NEWS STREAM


GLOBAL
COMPUTER CHIP SCARE
The bugs are known as 'Spectre' and 'Meltdown'
BBC WORLD NEWS
£:HK$ 10.58
EURO:£ 0.891


SECURITY FLAW REVEALED
Intel (Prev)
45.26
-1.59
[-3.39%]
Intel (After Hours)
44.85
-0.41
[-0.91%]
CAPITAL CONNECTION
SHROUT: ISSUE NOT UNIQUE TO INTEL, BUT IT'S AFFECTED THE MOST
CNBC

The Fallout

You realize it is something big when...

- it is in the news, all over the world
- you get a Wikipedia article in multiple languages

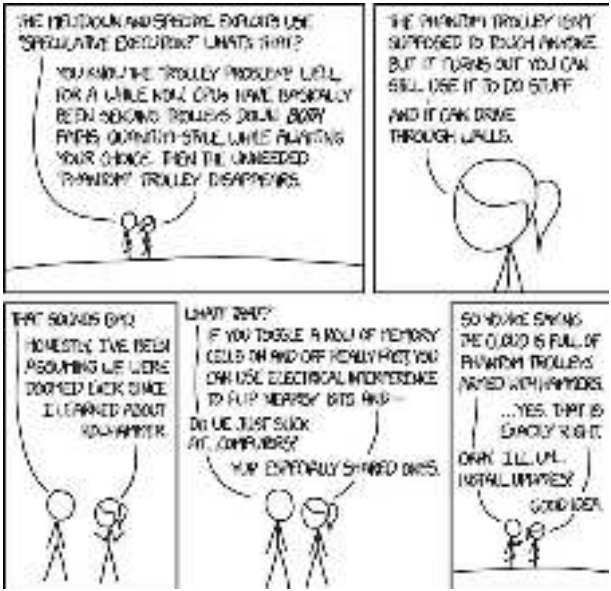

Wikipedia
The Free Encyclopedia
Article
Talk
Read
Edit
View history
Meltdown (security vulnerability)
From Wikipedia, the free encyclopedia
Meltdown is a hardware vulnerability affecting Intel x86 microprocessors and some ARM-based microprocessors.[1][2][3] It allows a rogue process to read all memory, even when it is not authorized to do so.
Meltdown affects a wide range of systems. At the time of disclosure, this included all devices running any but the most recent and patched versions of iOS,[4] Linux[5][6], macOS,[4] or Windows. Accordingly, many servers and cloud services were impacted,[7] as well as a potential majority of smart devices and embedded devices using ARM based processors (mobile devices, smart TVs and others), including a wide range of networking equipment. A purely software workaround to Meltdown has been assessed as slowing computers between 5 and 30 percent in certain specialized workloads,[8] although companies responsible for software correction of the exploit are reporting minimal impact from general benchmark testing.[9]
Meltdown was issued a Common Vulnerabilities and Exposures ID of CVE-2017-5754 or, also known as Rogue Data Cache Load,[7] in January 2018. It was disclosed in conjunction with another exploit, Spectre, with which it shares some, but not all, characteristics. The Meltdown and Spectre vulnerabilities are considered "catastrophic"
MELTDOWN
The logo used by the team that discovered the vulnerability

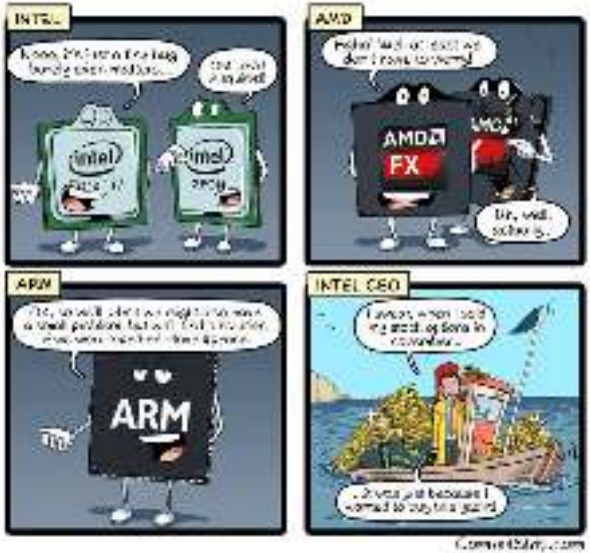

Wikipedia
The free encyclopedia
Article
Talk
Read
Edit
View history
Spectre (security vulnerability)
From Wikipedia, the free encyclopedia
Spectre is a vulnerability that affects modern microprocessors that perform branch prediction.[1][2][3] On most processors, the speculative execution resulting from a branch misprediction may leave observable side effects that may reveal private data to attackers. For example, if the pattern of memory accesses performed by such speculative execution depends on private data, the resulting state of the data cache constitutes a side channel through which an attacker may be able to extract information about the private data using a timing attack.[4][5][6]
Two Common Vulnerabilities and Exposures IDs related to Spectre, CVE-2017-5753 (bounds check bypass) and CVE-2017-5715 (branch target injection), have been issued.[7] JIT engines used for JavaScript were found vulnerable. A website can read data stored in the browser for another website, or the browser's memory itself.[8]
Several procedures to help protect home computers and related devices from the Spectre (and Meltdown) security vulnerabilities have been published.[9][10][11][12] Spectre patches have been reported to significantly slow down performance, especially on older computers; on the newer 8th generation Core platforms, benchmark performance drops of 2–14 percent have been measured.[13] Meltdown patches may also produce performance loss.[10][14][15] On January 18, 2018, unwanted reboots, even for newer Intel chips, due to
SPECTRE
A logo created for the vulnerability, featuring a ghost with a branch

The Fallout

You realize it is something big when...

- it is in the news, all over the world
- you get a Wikipedia article in multiple languages
- there are comics, including xkcd


THE INFLUXION AND SPECTRE EXPLOITS USE "SPECULATIVE EXECUTION" UNITS, RIGHT?
YOU KNOW THE "TROLLEY PROBLEM" WHERE, FOR A WHILE, ALL OTHA HAVE BASICALLY BEEN SECOND TROLLEYS DOING BORY PIPES DURATION-STYLE WHILE AWAITING YOUR CHOICE. THEN THE UNNEEDED PHANTOM TROLLEY DISAPPEARS.
THE PHANTOM TROLLEY ISN'T SUPPOSED TO TOUCH ANYONE, BUT IT TURNS OUT YOU CAN STILL USE IT TO DO STUFF.
AND IT CAN DRIVE THROUGH WALLS.
THAT SOUNDS BAD.
HONESTLY, I'VE BEEN ASSUMING WE WERE DOOMED EVER SINCE I LEARNED ABOUT ROWHAMMER.
WHAT, WHY?
IF YOU TOGGLE A BOU OF MEMORY CELLS ON AND OFF REALLY FAST YOU CAN USE ELECTRICAL INTERFERENCE TO FLIP NEARBY BITS AND—
DO WE JUST SUCK AT COMPUTERS?
YOUR EXPERTLY SHAPED BANS.
SO YOU'RE SAYING THE CLOUD IS FULL OF PHANTOM TROLLEYS NAMED WITH HAMMERS.
...YES. THAT IS EXACTLY RIGHT.
OKAY, I'LL UPL INSTALL UMMYEX.
GOOD IDEA.


INTEL
intel
intel
AMD
AMD
FX
ARM
ARM
INTEL CEO

You realize it is something big when...

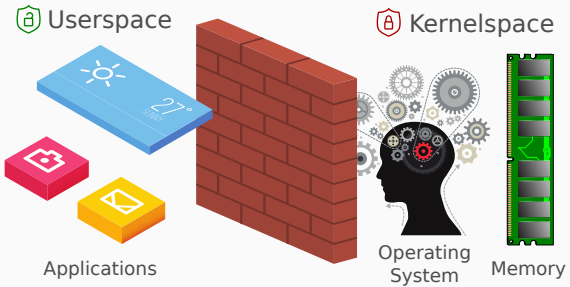
- it is in the news, all over the world
- you get a Wikipedia article in multiple languages
- there are comics, including xkcd
- you get a lot of Twitter follower after Snowden mentioned you


Edward Snowden
You may have heard about @Intel's horrific Meltdown bug. But have you watched it in action? When your computer asks you to apply updates this month, don't click "not now."
& @misc0110)

The Wall

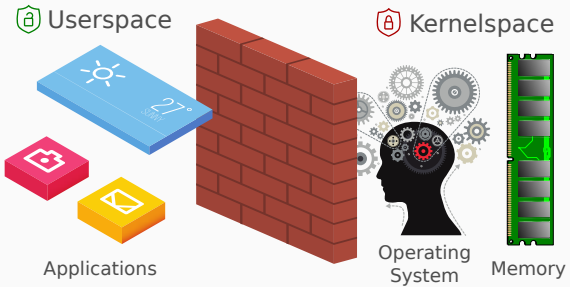
The Core of Meltdown/Spectre

- Kernel is isolated from user space



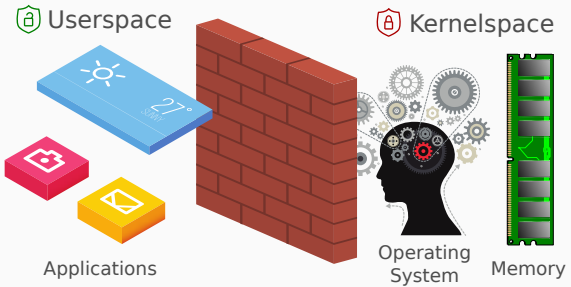
The Core of Meltdown/Spectre

- Kernel is isolated from user space
- This isolation is a combination of hardware and software



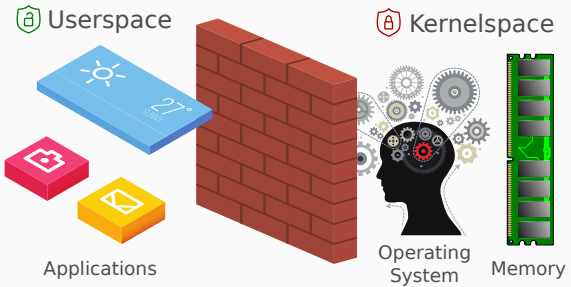
The Core of Meltdown/Spectre

- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel



The Core of Meltdown/Spectre

- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel
- There is only a well-defined interface → syscalls



1337 4242

FOOD CACHE

Revolutionary concept!

Store your food at home, never go to the grocery store during cooking.

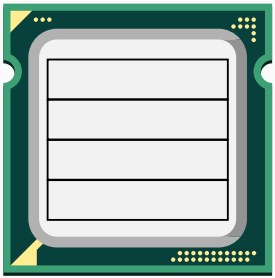
Can store **ALL** kinds of food.

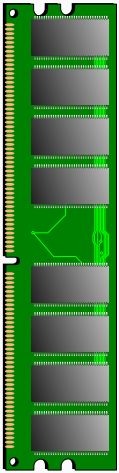
ONLY TODAY INSTEAD OF ~~$1,300~~

$1,299

ORDER VIA PHONE: +555 12345

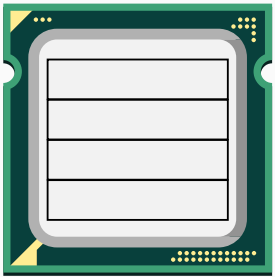
```
printf("%d", i);
printf("%d", i);
```

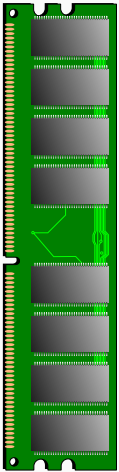




```
printf("%d", i);
printf("%d", i);
```

Cache miss





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printf("%d", i);
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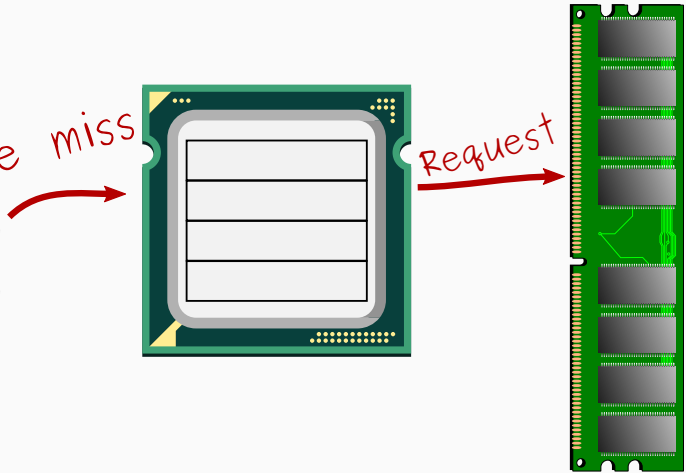

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printf("%d", i);
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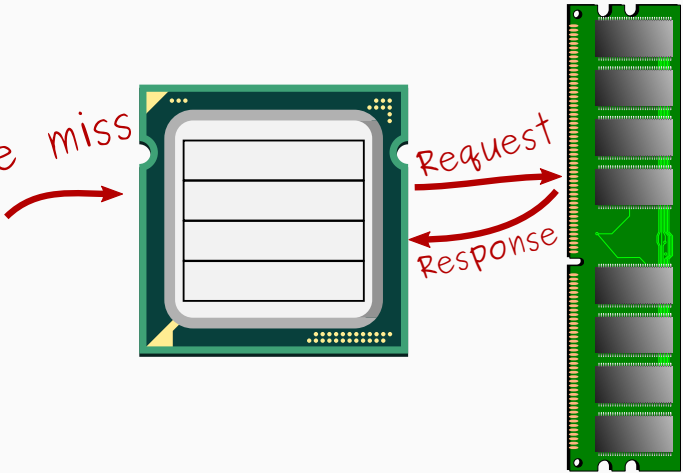

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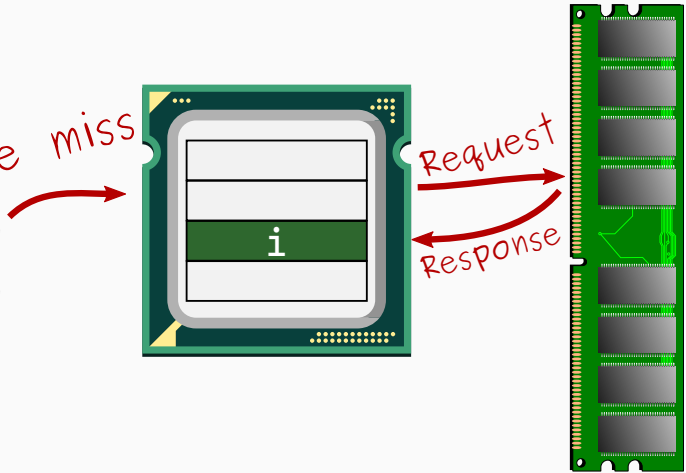
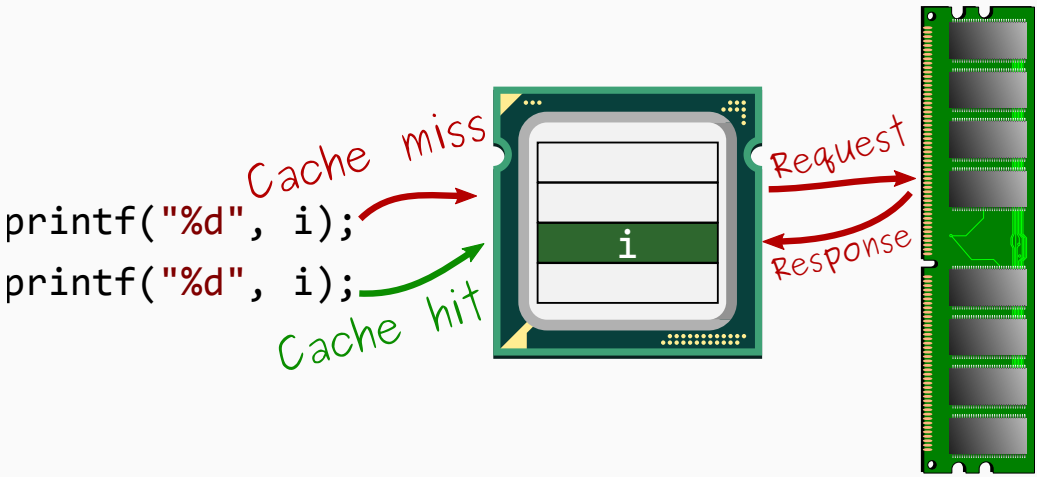
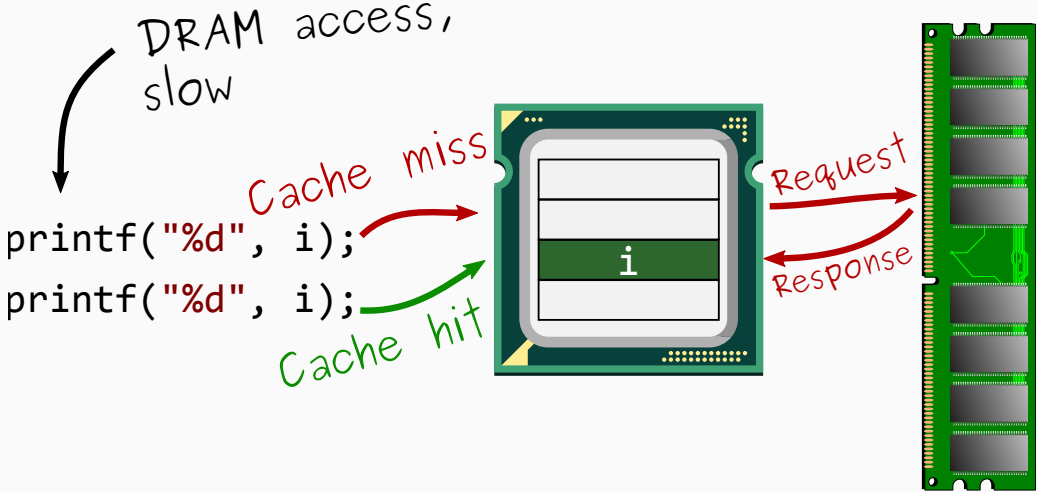
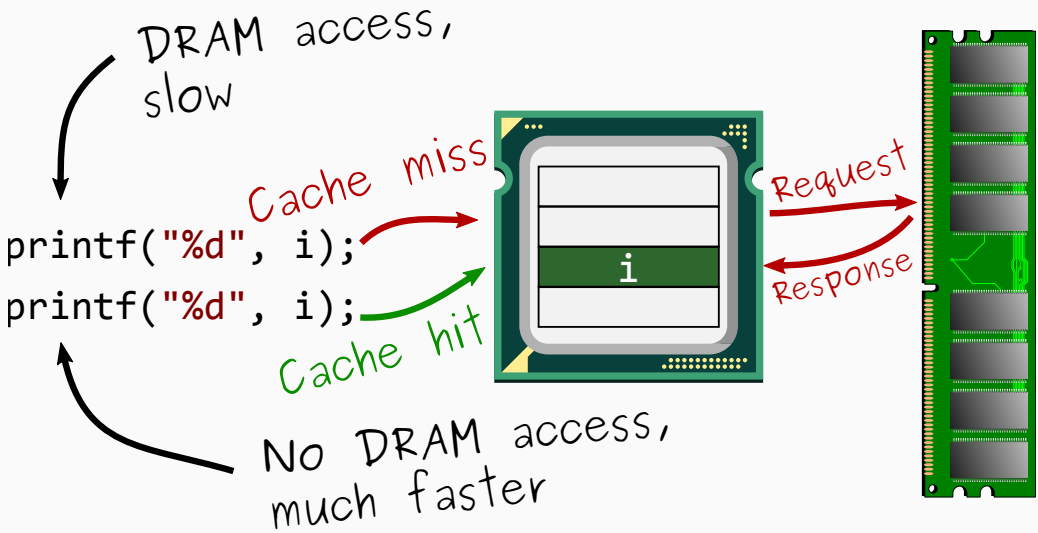



printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response


DRAM access, slow
printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response

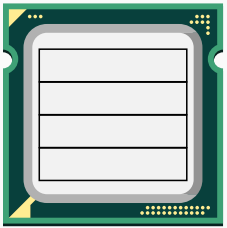

DRAM access,
slow
printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response
No DRAM access,
much faster

Shared Memory

ATTACKER

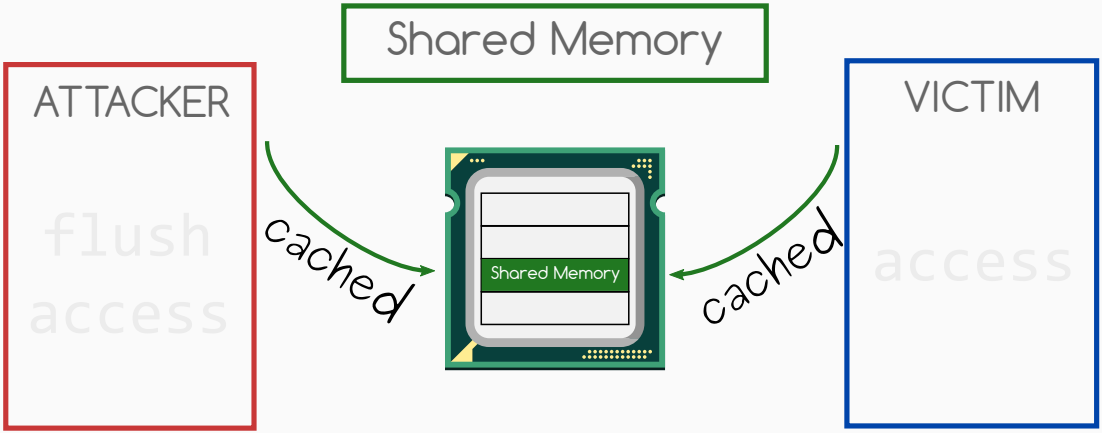
flush

access



VICTIM

access

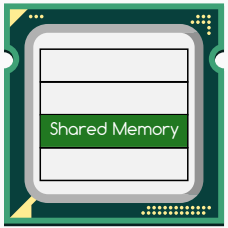

Shared Memory
ATTACKER
flush
access
cached
Shared Memory
cached
VICTIM
access

Shared Memory

ATTACKER

flush

access



VICTIM

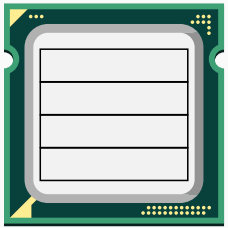
access

Shared Memory

ATTACKER

flush

access



VICTIM

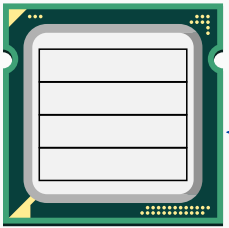
access

Shared Memory

ATTACKER

flush

access



VICTIM

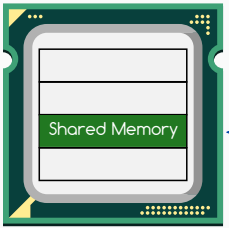
access

Shared Memory

ATTACKER

flush

access



VICTIM

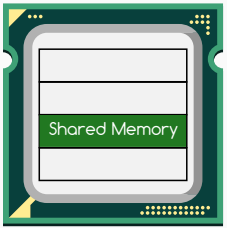
access

Shared Memory

ATTACKER

flush

access



VICTIM

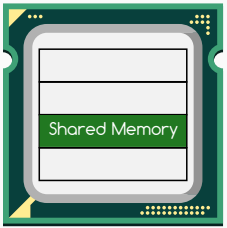
access

Shared Memory

ATTACKER

flush

access

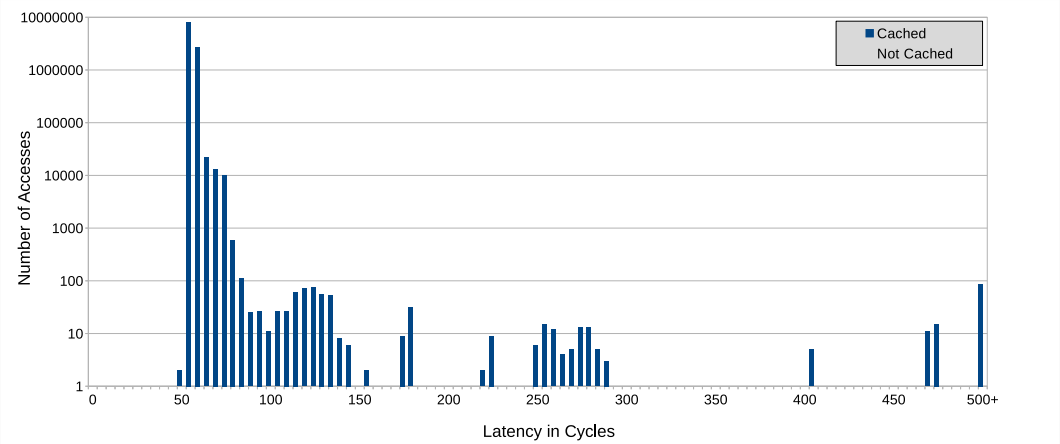


VICTIM

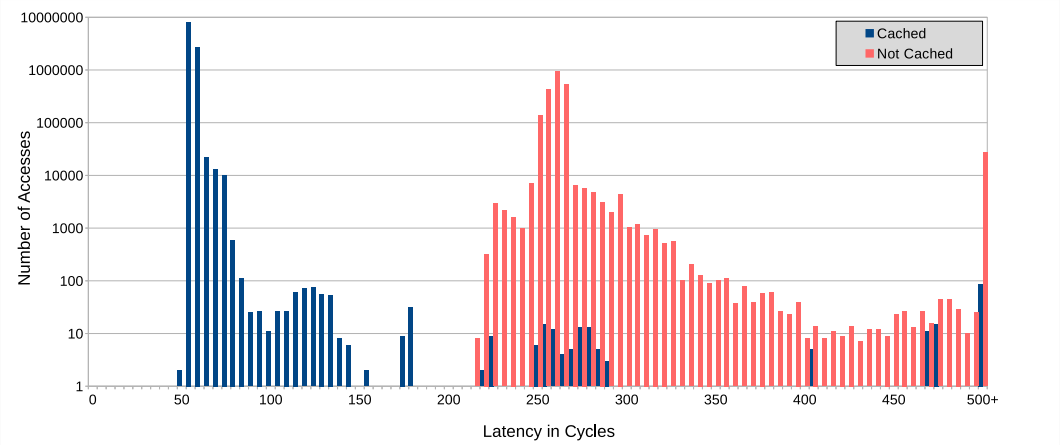
access

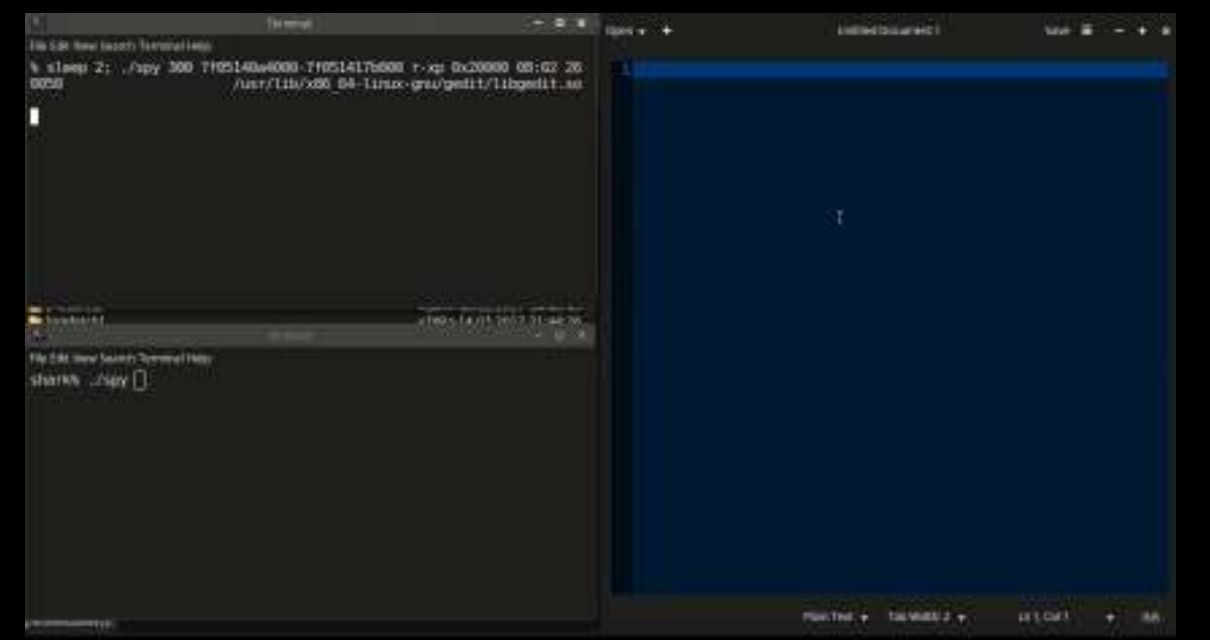
fast if victim accessed data,
slow otherwise

Memory Access Latency

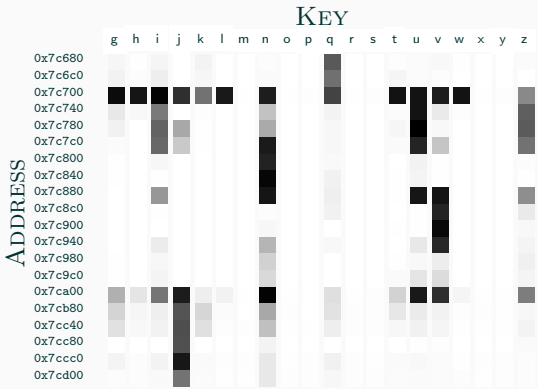


Memory Access Latency





Cache Template Attack Demo


KEY
g h i j k l m n o p q r s t u v w x y z
ADDRESS
0x7c680
0x7c6c0
0x7c700
0x7c740
0x7c780
0x7c7c0
0x7c800
0x7c840
0x7c880
0x7c8c0
0x7c900
0x7c940
0x7c980
0x7c9c0
0x7ca00
0x7cb80
0x7cc40
0x7cc80
0x7ccc0
0x7cd00


Back to Work

7. Serve with cooked and peeled potatoes

Wait for an hour

Wait for an hour

LATENCY

1. Wash and cut vegetables

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

4. Fry vegetables until golden and softened

1. Wash and cut vegetables

2. Pick the basil leaves and set aside

3. Heat 2 tablespoons of oil in a pan

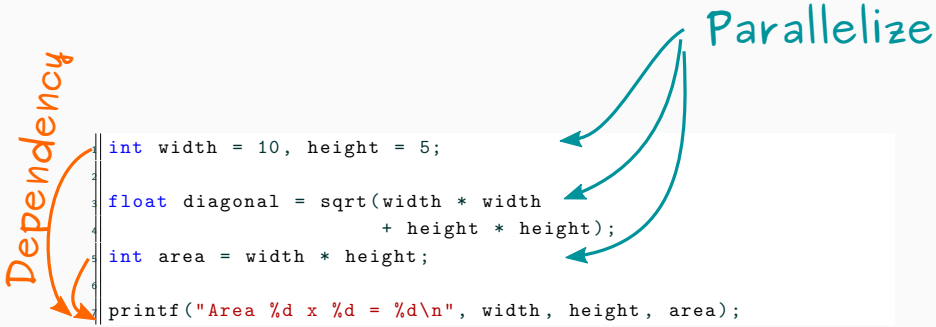
4. Fry vegetables until golden and softened

Dependency

Parallelize

Out-of-order Execution

```
1 int width = 10, height = 5;
2
3 float diagonal = sqrt(width * width
4                       + height * height);
5 int area = width * height;
6
7 printf("Area %d x %d = %d\n", width, height, area);
```




```
1 int width = 10, height = 5;
2
3 float diagonal = sqrt(width * width
4                      + height * height);
5 int area = width * height;
6
7 printf("Area %d x %d = %d\n", width, height, area);
```

```
1 char data = *(char*)0xffffffff81a000e0;
2 printf("%c\n", data);
```

```
1 char data = *(char*)0xffffffff81a000e0;
2 printf("%c\n", data);
```

```
1 segfault at ffffffff81a000e0 ip 0000000000400535
2       sp 00007ffce4a80610 error 5 in reader
```

```
1 char data = *(char*)0xffffffff81a000e0;
2 printf("%c\n", data);
```

```
1 segfault at ffffffff81a000e0 ip 0000000000400535
2       sp 00007ffce4a80610 error 5 in reader
```

- Kernel addresses are not accessible

```
1 char data = *(char*)0xffffffff81a000e0;
2 printf("%c\n", data);
```

```
1 segfault at ffffffff81a000e0 ip 0000000000400535
2       sp 00007ffce4a80610 error 5 in reader
```

- Kernel addresses are not accessible
- Are privilege checks also done when executing instructions out of order?

- Adapted code

```
1 *(volatile char*)0;
2 array[84 * 4096] = 0; // unreachable
```

- Adapted code

```
1 *(volatile char*)0;
2 array[84 * 4096] = 0; // unreachable
```

- Static code analyzer is not happy

```
1 warning: Dereference of null pointer
2         *(volatile char*)0;
```

- Flush+Reload over all pages of the array

- "Unreachable" code line was actually executed

- Flush+Reload over all pages of the array

- "Unreachable" code line was actually executed
- Exception was only thrown afterwards

- Combine the two things

```
char data = *(char*)0xffffffff81a000e0;
array[data * 4096] = 0;
```

- Combine the two things

```
1 char data = *(char*)0xffffffff81a000e0;
2 array[data * 4096] = 0;
```

= sending end of a cache covert channel

- Then check whether any part of `array` is cached

- Combine the two things

```
1 char data = *(char*)0xffffffff81a000e0;
2 array[data * 4096] = 0;
```

  = sending end of a cache covert channel

- Then check whether any part of `array` is cached

  = receiving end of a cache covert channel

- Flush+Reload over all pages of the array

- Index of cache hit reveals data

- Flush+Reload over all pages of the array

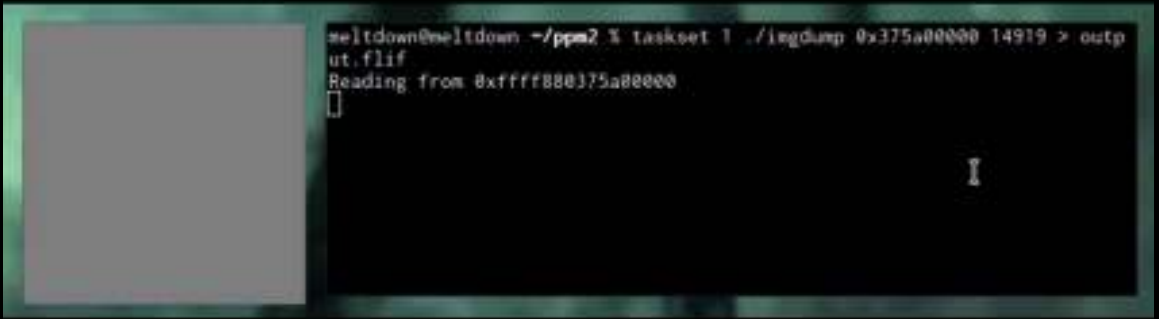
- Index of cache hit reveals data
- Permission check is in some cases not fast enough

Terminal

File Edit View Search Terminal Help

```
mschwarz@lab06:~/Documents$
```


CAN YOU
ENHANCE THAT


meltdown@meltdown ~/ppm2 % taskset 1 ./imgdump 0x375a00000 14919 > outp
ut.flif
Reading from 0xffff880375a00000

Leaking Passwords from your Password Manager


AND IN OTHER NEWS...
MELTDOWN
WE'RE ALL DOOMED, SANDRA.
HOW ABOUT THE WEATHER?

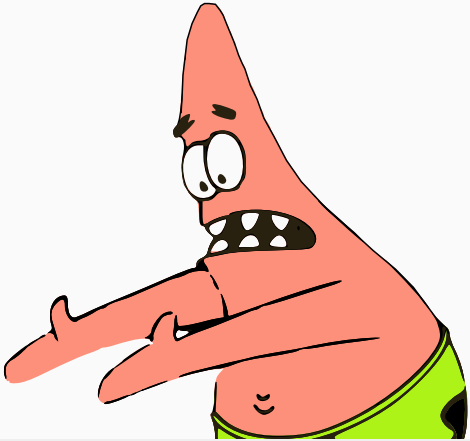
Not so fast...

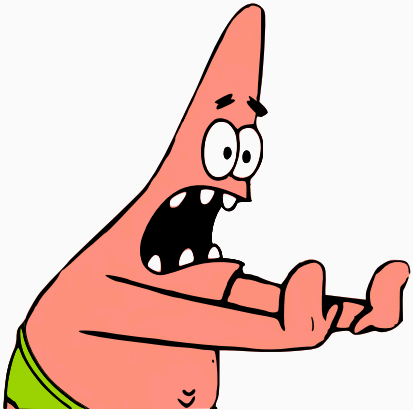
Take the kernel addresses...

- Kernel addresses in user space are a problem

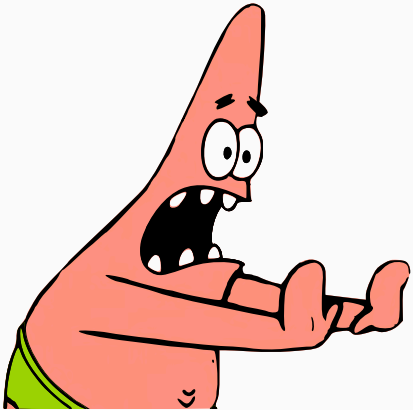
Take the kernel addresses...

- Kernel addresses in user space are a problem
- Why don't we take the kernel addresses...





- ...and remove them if not needed?



- ...and remove them if not needed?
- User accessible check in hardware is not reliable

Idea

- Let's just unmap the kernel in user space

Idea

- Let's just unmap the kernel in user space
- Kernel addresses are then no longer present

Idea

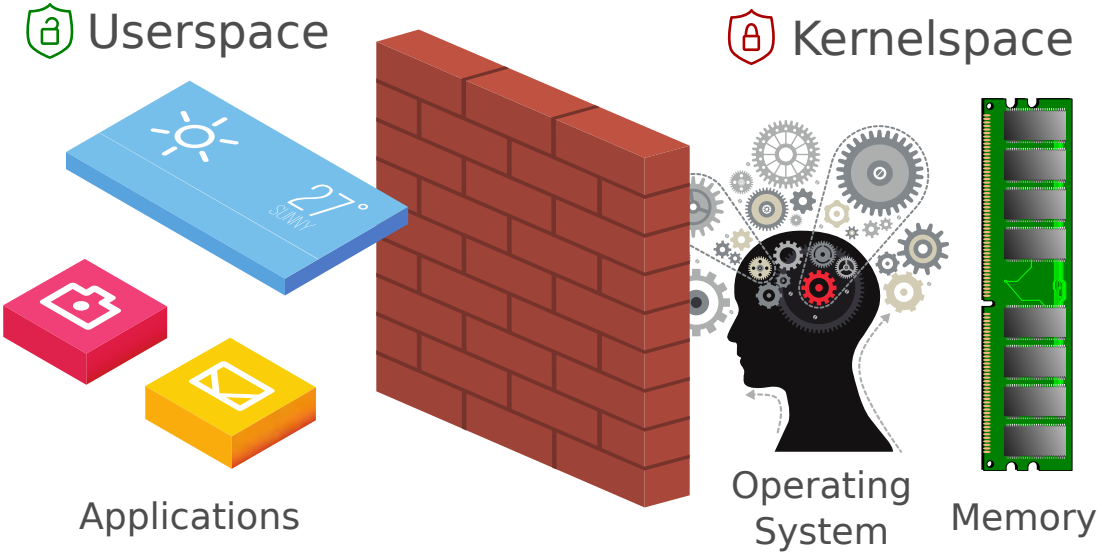
- Let's just unmap the kernel in user space
- Kernel addresses are then no longer present
- Memory which is not mapped cannot be accessed at all


Kernel Address Isolation to have Side channels Efficiently Removed

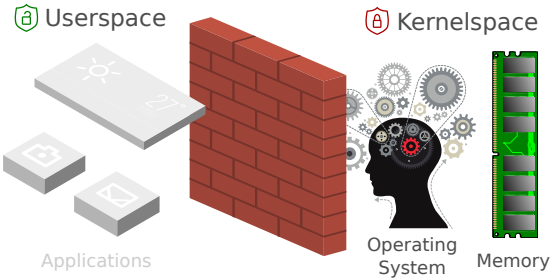
KAISER /ˈkʌɪzə/

1. [german] Emperor, ruler of an empire
2. largest penguin, emperor penguin

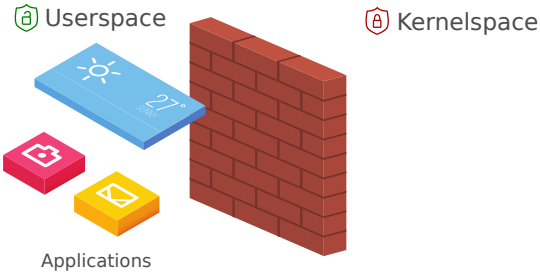
Kernel **A**ddress **I**solation to have **S**ide channels **E**fficiently **R**emoved

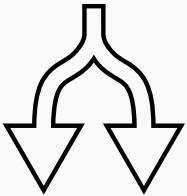

Userspace
Kernelspace
27°
Applications
Operating System
Memory

Kernel View

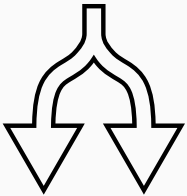


User View

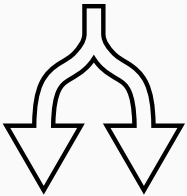




- We published KAISER in July 2017



- We published KAISER in July 2017
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)



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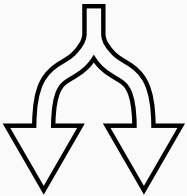

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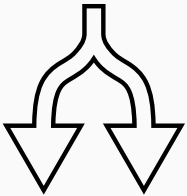
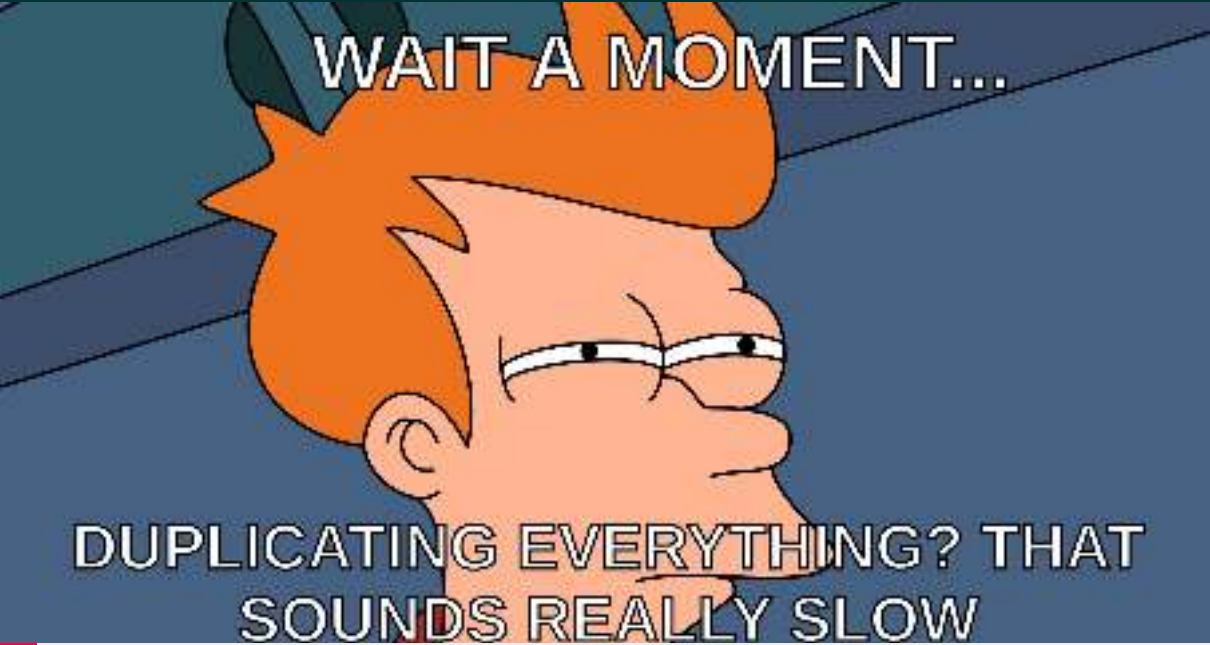
- Apple implemented it in macOS 10.13.2 and called it "Double Map"



- We published KAISER in July 2017
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it "Double Map"
- All share the same idea: switching address spaces on context switch


WAIT A MOMENT...
DUPLICATING EVERYTHING? THAT SOUNDS REALLY SLOW

Performance

- Depends on how often you need to switch between kernel and user space

Performance

- Depends on how often you need to switch between kernel and user space
- Can be slow, 40% or more on old hardware

Performance

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- But modern CPUs have additional features

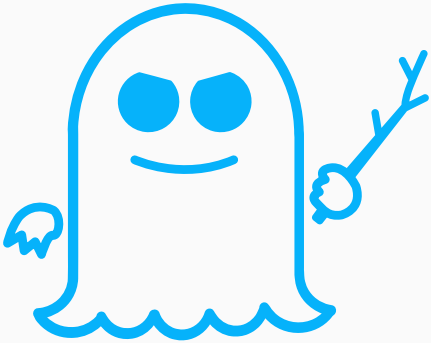
Performance

- Depends on how often you need to switch between kernel and user space
- Can be slow, 40% or more on old hardware
- But modern CPUs have additional features
- $\Rightarrow$ Performance overhead on average below 2%

MELTDOWN

SPECTRE

MELTDOWN

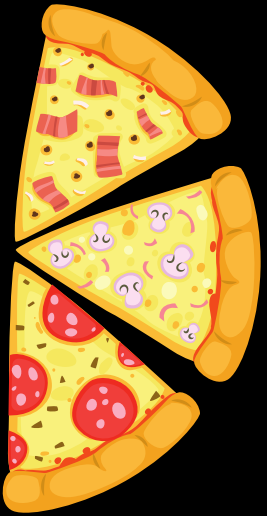


SPECTRE

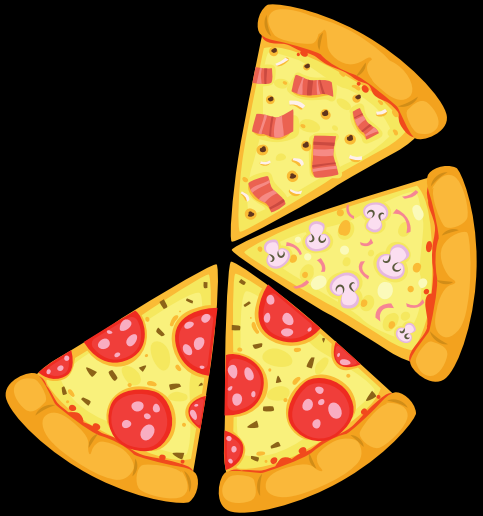

PIZZA
SPECIAL RECIPES

Prosciutto

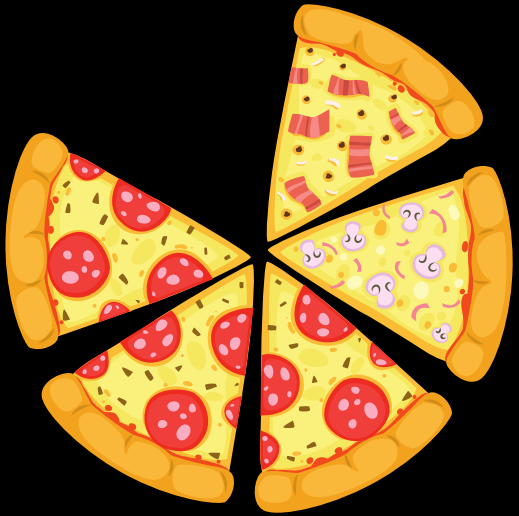
Funghi



Diavolo



Diavolo



Diavolo

Diavolo


»A table for 6 please«

Speculative Cooking


»A table for 6 please«


PIZZA
SPECIAL RECIPES


Pizza


Pizza

What does Spectre do?

- Mistrains branch prediction

What does Spectre do?

- Mistrains branch prediction
- CPU speculatively executes code which should not be executed

What does Spectre do?

- Mistrains branch prediction
- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls

What does Spectre do?

- Mistrains branch prediction
- CPU speculatively executes code which should not be executed
- Can also mistrain indirect calls

→ Spectre “convinces” program to execute code

```
index = 0;

char* data = "textKEY";

if (index < 4)
```

```
index = 0;
```

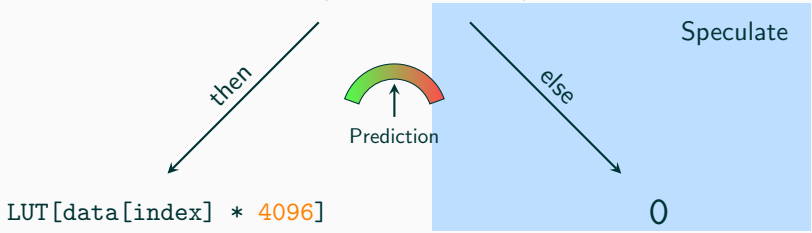
```
char* data = "textKEY";
```

```
if (index < 4)
```

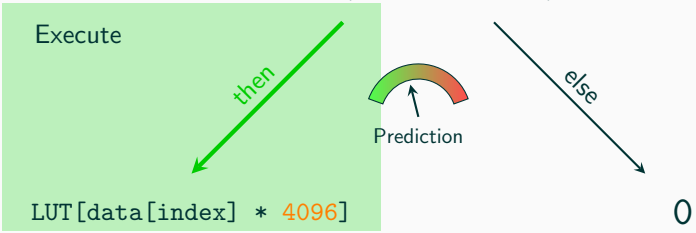
```
index = 0;
```

```
char* data = "textKEY";
```

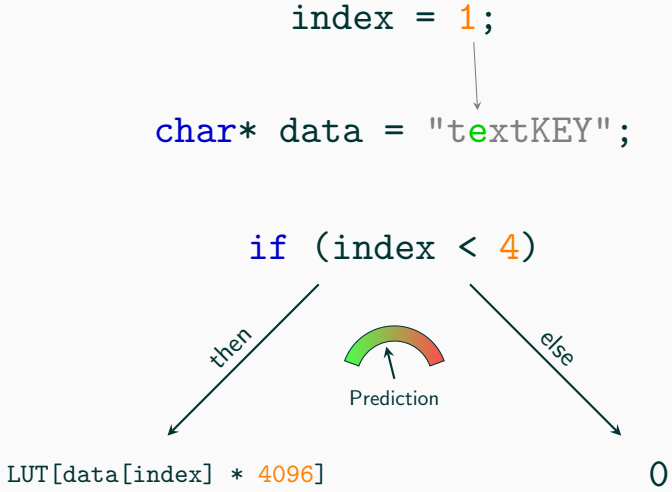
```
if (index < 4)
```



```
index = 0;
char* data = "textKEY";
if (index < 4)
```



```
index = 1;

char* data = "textKEY";

if (index < 4)
```

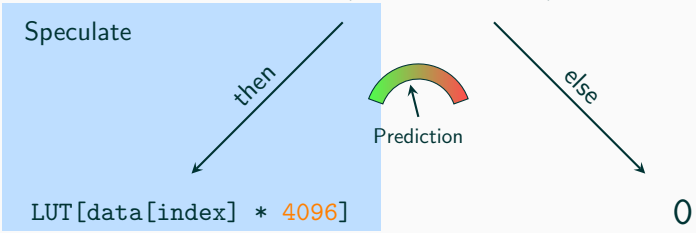

index = 1;
char* data = "textKEY";
if (index < 4)
then
else
Prediction
LUT[data[index] * 4096]
0

Spectre (variant 1)

```
index = 1;
```

```
char* data = "textKEY";
```

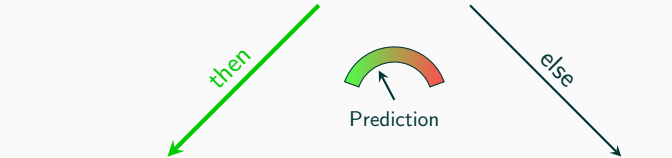
```
if (index < 4)
```



```
index = 1;
```

```
char* data = "textKEY";
```

```
if (index < 4)
```

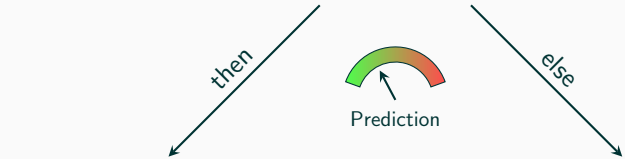


```
index = 2;

char* data = "textKEY";

if (index < 4)
```

```
index = 2;
```

```
char* data = "textKEY";
```

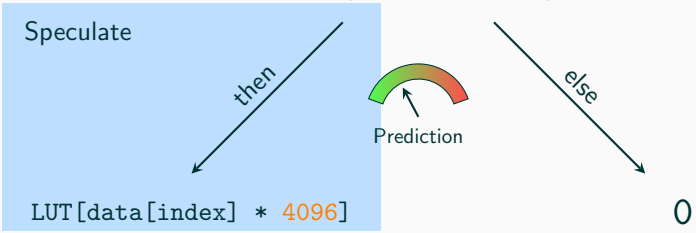
```
if (index < 4)
```

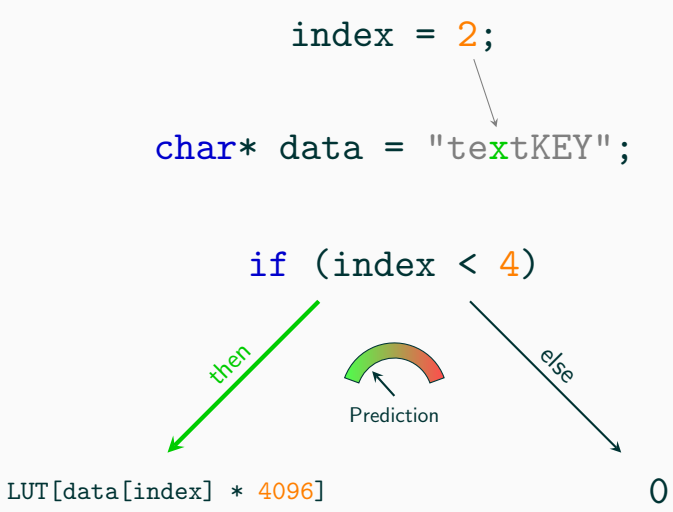


```
index = 2;
```

```
char* data = "textKEY";
```

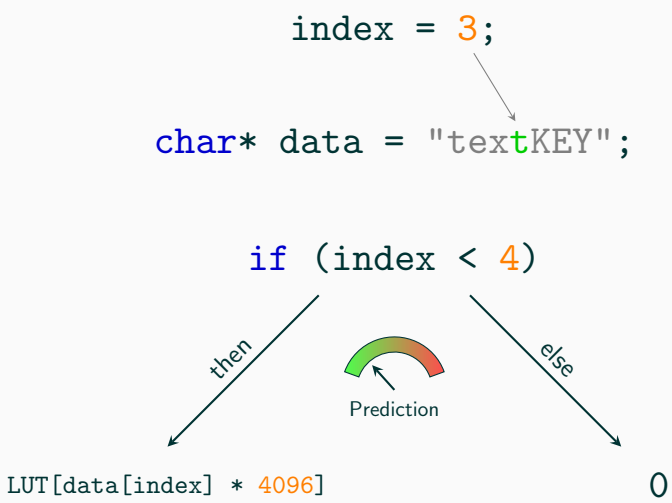
```
if (index < 4)
```




index = 2;
char* data = "textKEY";
if (index < 4)
then
Prediction
else
LUT[data[index] * 4096]
0

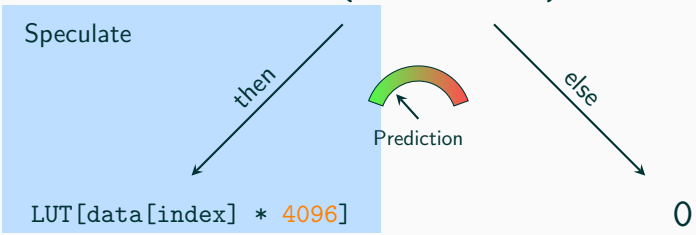
```
index = 3;

char* data = "textKEY";

if (index < 4)
```

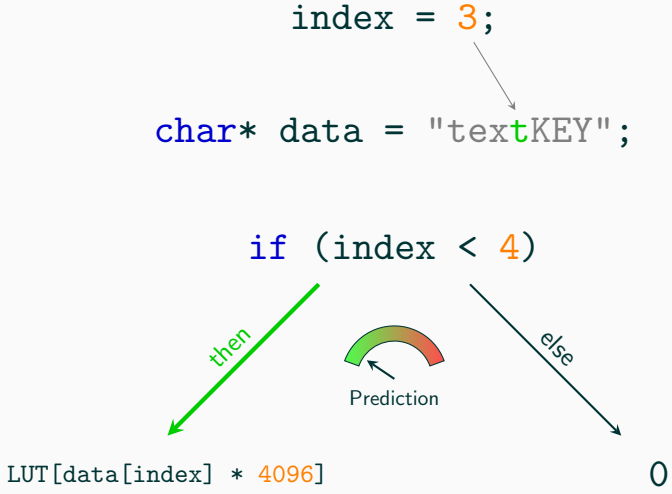
`LUT[data[index] * 4096]` 0


index = 3;
char* data = "textKEY";
if (index < 4)
then
else
Prediction
LUT[data[index] * 4096]
0

Spectre (variant 1)

```
index = 3;
char* data = "textKEY";
if (index < 4)
```




index = 3;
char* data = "textKEY";
if (index < 4)
then
Prediction
else
LUT[data[index] * 4096]
0

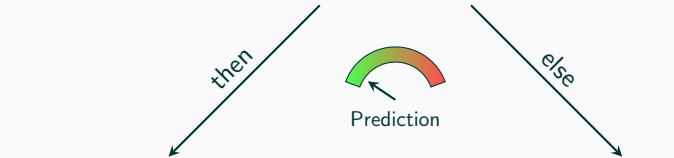
```
index = 4;

char* data = "textKEY";

if (index < 4)
```

Spectre (variant 1)

```
index = 4;
```

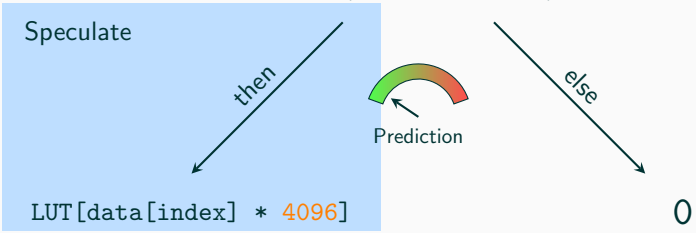
```
char* data = "textKEY";
```

```
if (index < 4)
```



Spectre (variant 1)

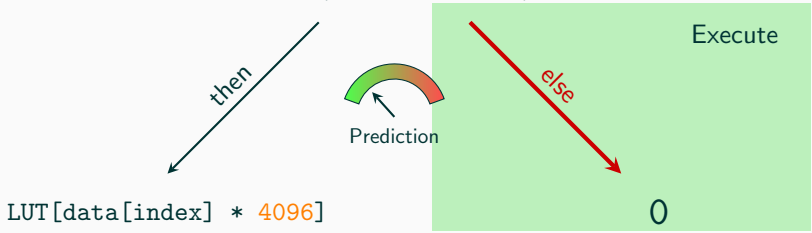
```
index = 4;

char* data = "textKEY";

if (index < 4)
```



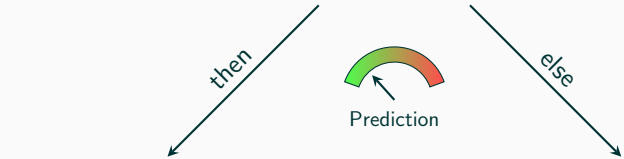
```
index = 4;
```

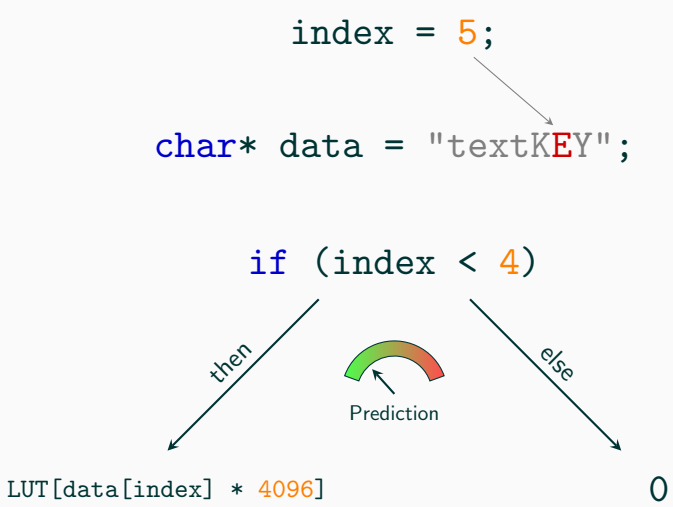
```
char* data = "textKEY";
```

```
if (index < 4)
```



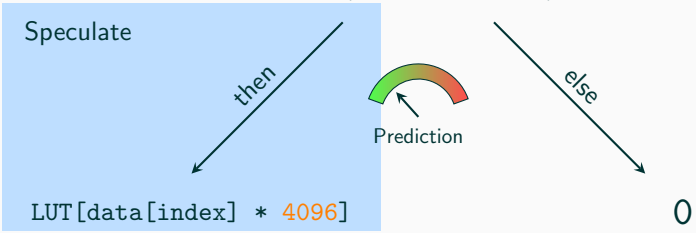
```
index = 5;

char* data = "textKEY";

if (index < 4)
```



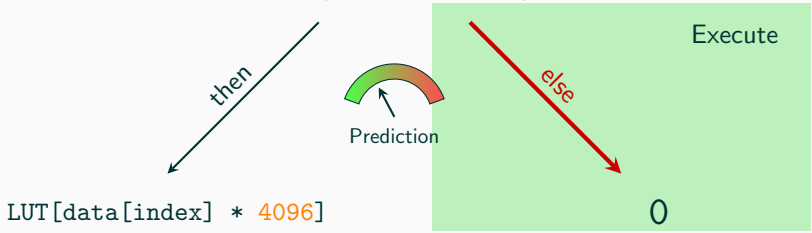

index = 5;
char* data = "textKEY";
if (index < 4)
then
Prediction
else
LUT[data[index] * 4096]
0

Spectre (variant 1)

```
index = 5;

char* data = "textKEY";

if (index < 4)
```



```
index = 5;

char* data = "textKEY";

if (index < 4)
```



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index = 6;

char* data = "textKEY";

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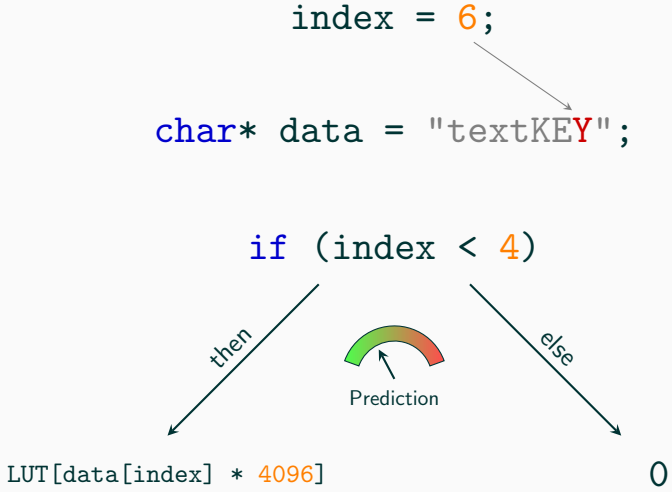
index = 6;
char* data = "textKEY";
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then
Prediction
else
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Spectre (variant 1)

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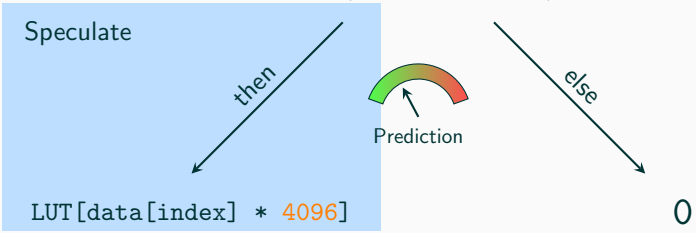

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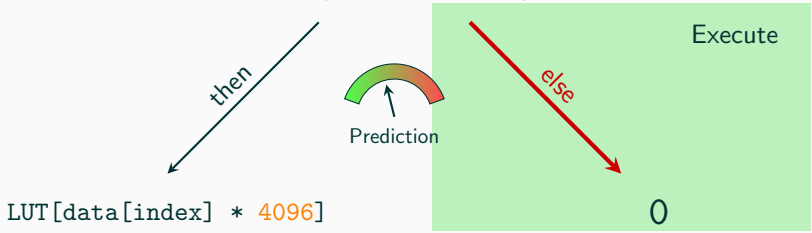

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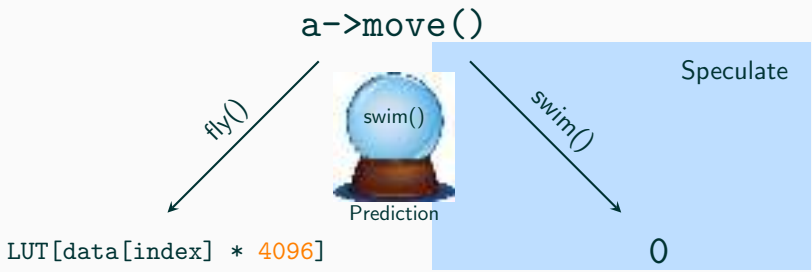

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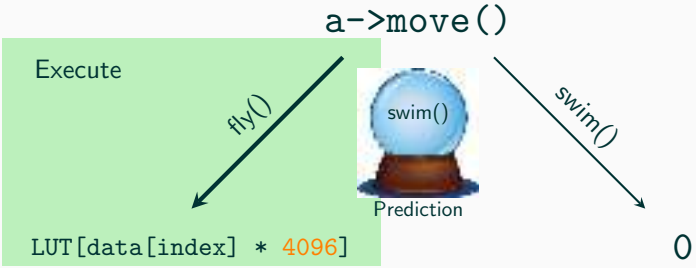

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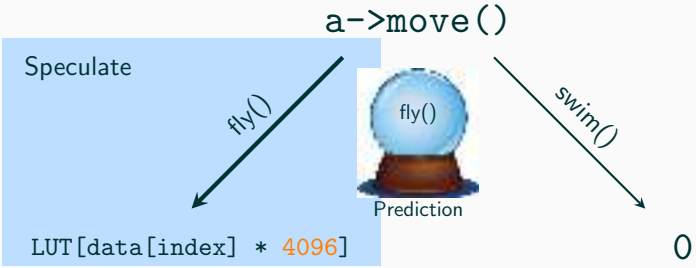

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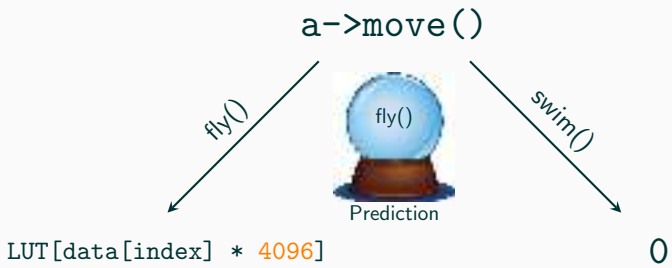

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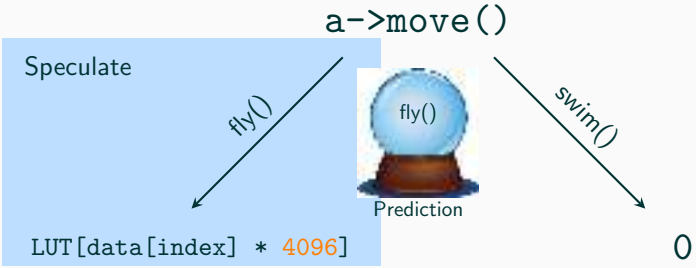

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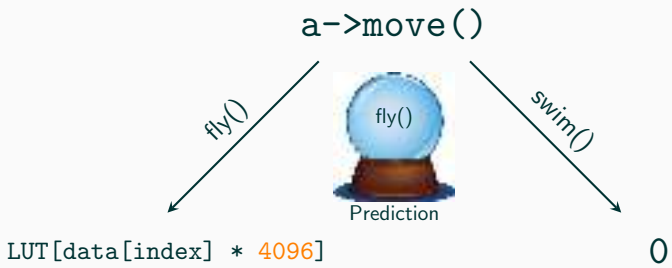

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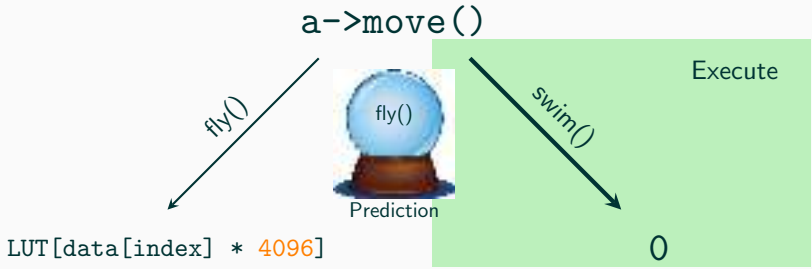

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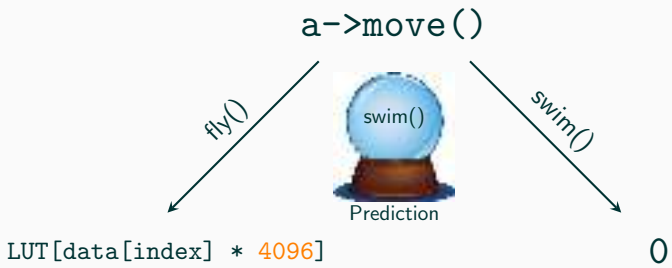

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- Also: How to disable it?
- Speculative execution is deeply integrated into CPU


GHOSTBUSTERS

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Spectre Variant 1 Mitigations

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- x86: `LFENCE`, ARM: `CSDB`

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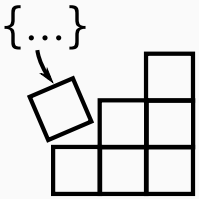
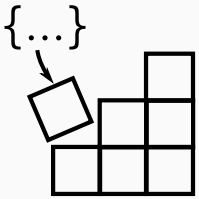
- x86: `LFENCE`, ARM: `CSDB`
- Available on all Intel CPUs, retrofitted to existing ARMv7 and ARMv8





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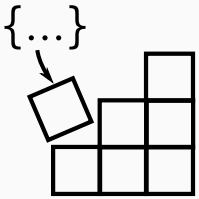

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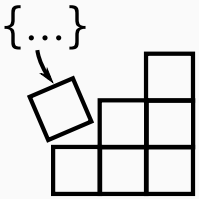

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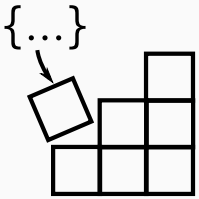

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- Explicit use by programmer: `__builtin_load_no_speculate`

Spectre Variant 1 Mitigations

```
// Unprotected

...r array[9];

int get_value(unsigned int a) {
  int tmp;

  if (a < 9) {
    tmp = array[a];
  } else {
    tmp = FAIL;
  }

  return tmp;
}
```

Spectre Variant 1 Mitigations

```
// Unprotected

int array[N];

int get_value(unsigned int n) {
  int tmp;

  if (n < N) {
    tmp = array[n];
  } else {
    tmp = FAIL;
  }

  return tmp;
}
```

```
// Protected

int array[N];

int get_value(unsigned int n) {

  int *lower = array;
  int *ptr = array + n;
  int *upper = array + N;

  return
    __builtin_load_no_speculate
    (ptr, lower, upper, FAIL);

}
```


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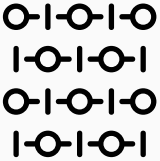

Intel released microcode updates

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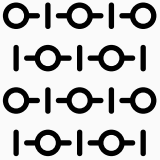

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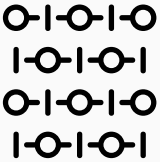

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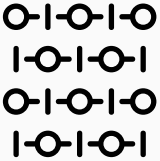

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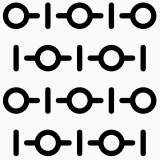

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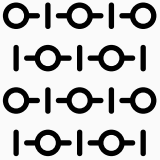

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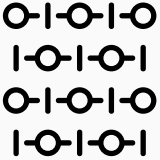

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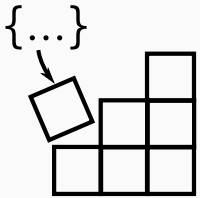
Retpoline (compiler extension)



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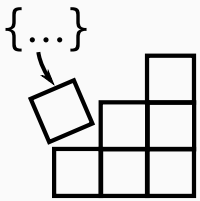

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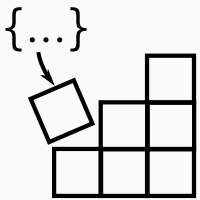

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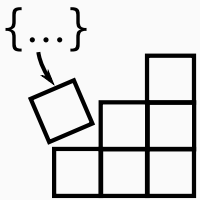

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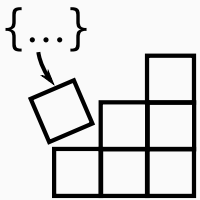

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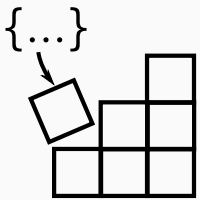

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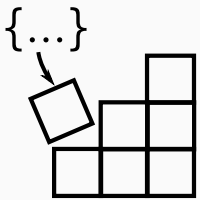

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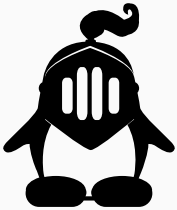

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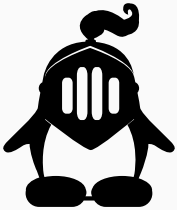
Spectre Variant 2 Mitigations (Software)



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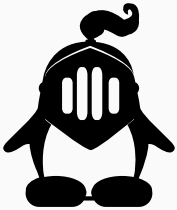

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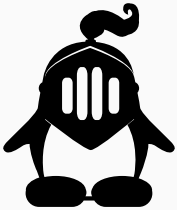

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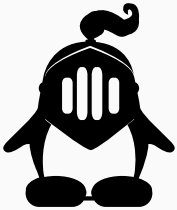

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→ Spectre works on secure enclaves

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- in theory: OoO not required, pipelining can be sufficient

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- fundamentally builds on branch (mis)prediction
- turning off speculative execution entirely would work
- has nothing to do with the `user_accessible`-bit
- KAISER has no effect on Spectre at all

Meltdown vs. Spectre

Meltdown

- Out-of-Order Execution
- has nothing to do with branch prediction
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→ melts down the isolation provided by the `user_accessible`-bit

- in theory: OoO not required, pipelining can be sufficient
- mitigated by KAISER

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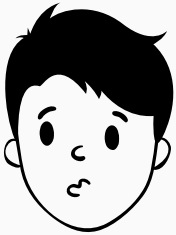
→ two papers, two names, etc.

But ...



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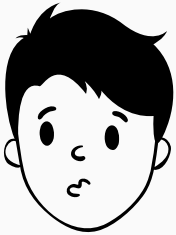

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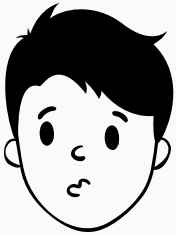

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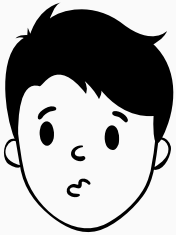

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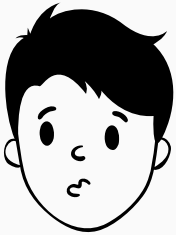

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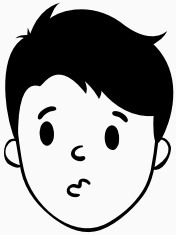

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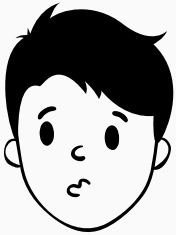

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What do we learn from it?

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→ for years we solely optimized for performance

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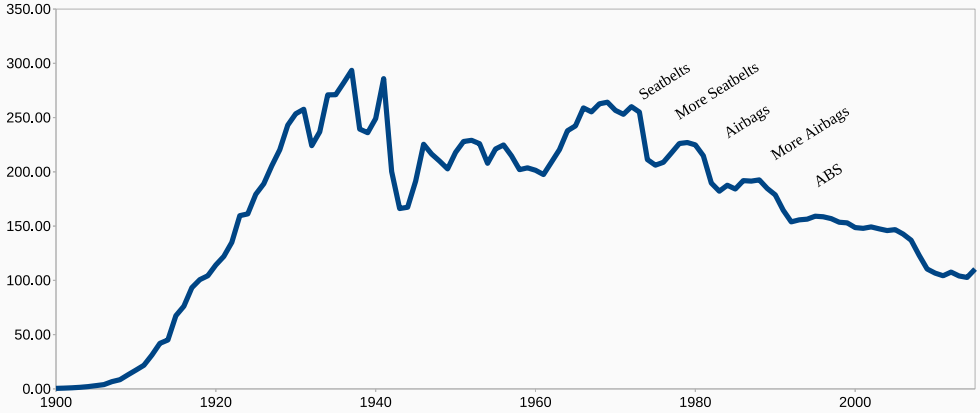

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Software-based Microarchitectural Attacks

Daniel Gruss

April 19, 2018

Graz University of Technology