

Brief Overview on Meltdown and Spectre

Daniel Gruss

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Graz University of Technology



- Daniel Gruss
- Post-Doc @ Graz University of Technology
- Twitter: @lavados
- Email: daniel.gruss@iaik.tugraz.at

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- secrets can leak through side channels

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- secrets can leak through side channels
- software-based \rightarrow no physical access





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- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel
- There is only a well-defined interface → syscalls





printf(<mark>"%d</mark>", i);

printf("%d", i);













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CPU Cache



CPU Cache























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Cache Template Attack Demo

Cache Template







• Out-of-order instructions leave microarchitectural traces



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- Out-of-order instructions leave microarchitectural traces
- We can see them for example in the cache
- Give such instructions a name: transient instructions
- We can indirectly observe the execution of transient instructions



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- ...or it is only done when commiting them



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- ...or it is only done when commiting them
- Add another layer of indirection to test

• Then check whether any part of array is cached



• Flush+Reload over all pages of the array



• Index of cache hit reveals data



• Flush+Reload over all pages of the array



- Index of cache hit reveals data
- Permission check is in some cases not fast enough



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• Kernel addresses in user space are a problem





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- Let's just unmap the kernel in user space





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- Let's just unmap the kernel in user space
- Kernel addresses are then no longer present
- Memory which is not mapped cannot be accessed at all

Today's operating systems:



Stronger kernel isolation:





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- We published KAISER in July 2017
- Intel and others improved and merged it into Linux as KPTI (Kernel Page Table Isolation)
- Microsoft implemented similar concept in Windows 10
- Apple implemented it in macOS 10.13.2 and called it "Double Map"
- All share the same idea: switching address spaces on context switch



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- But modern CPUs have additional features
- ullet \Rightarrow Performance overhead on average below 2%

Meltdown and Spectre







Meltdown and Spectre





SPECTRE

index =
$$0;$$





Spectre (variant 1)





index =
$$1;$$









index =
$$2;$$



Spectre (variant 1)








index =
$$3;$$











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index =
$$4;$$









index =
$$5;$$









index =
$$6;$$





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Animal* a = fish;







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- Much harder to fix, KAISER does not help
- Ongoing effort to patch via microcode update and compiler extensions

Spectre Variant 1 Mitigations



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 $\rightarrow\,$ speculation barrier to insert after every bounds check

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- $\rightarrow\,$ speculation barrier to insert after every bounds check
 - implemented as a compiler extension





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- Single Thread Indirect Branch Predictors (STIBP)
 - do not speculate based on anything the other hyperthread does
- Indirect Branch Predictor Barrier (IBPB):
 - flush branch-target buffer





```
push <call_target>
call 1f
2: ; speculation will continue here
lfence ; speculation barrier
jmp 2b ; endless loop
1:
lea 8(%rsp), %rsp ; restore stack pointer
ret ; the actual call to <call_target>
```

 $\rightarrow\,$ always predict to enter an endless loop



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attacks on crypto



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- $\bullet\,$ attacks on crypto $\rightarrow\,$ "software should be fixed"
- \bullet attacks on ASLR \rightarrow "ASLR is broken anyway"
- \bullet attacks on SGX and TrustZone \rightarrow "not part of the threat model"
- $\rightarrow\,$ for years we solely optimized for performance



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• the side channels were documented in the Intel manual



After learning about a side channel you realize:

- the side channels were documented in the Intel manual
- only now we understand the implications



Motor Vehicle Deaths in U.S. by Year

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A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)
- find good trade-offs between security and performance



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