Mitigation Plans for Microarchitectural Attacks

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July 15, 2019

Graz University of Technology

amazon.com
Prime+Probe

ANOTHER FLIP IN THE ROW

ROWHAMMER.JS

FANTASTIC TIMERS

AND WHERE TO FIND THEM

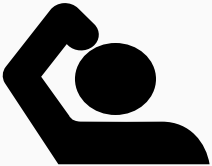
HIGH-RESOLUTION MICROARCHITECTURAL ATTACKS IN JAVASCRIPT

JavaScript zero

REAL JavaScript AND ZERO SIDE-CHANNEL ATTACKS

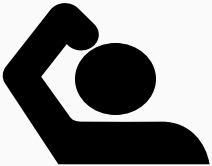

side channel
= obtaining meta-data and
deriving secrets from it
CHANGE MY MIND

Side Channel or not?



Side Channel or not?

- Observing cache utilization with performance counters?



Side Channel or not?

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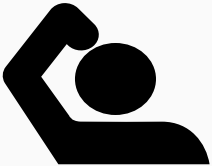

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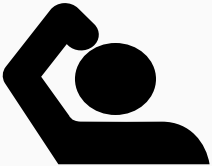

- Observing cache utilization with performance counters? → No
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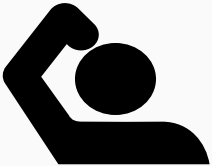

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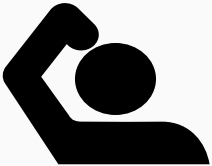

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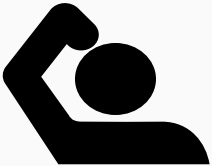
Side Channel or not?



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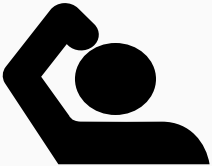

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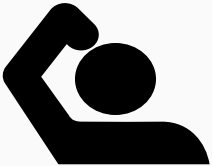

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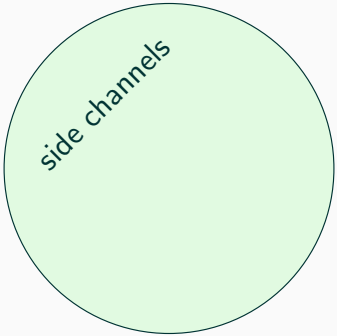
Speculative Side-Channel Attacks?



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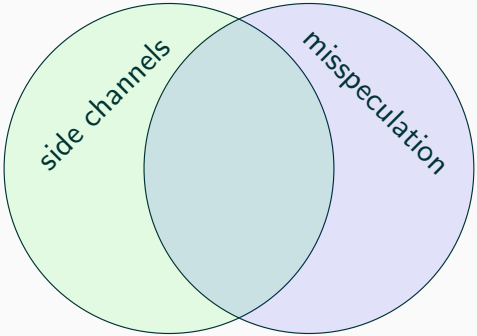
Speculative Side-Channel Attacks?



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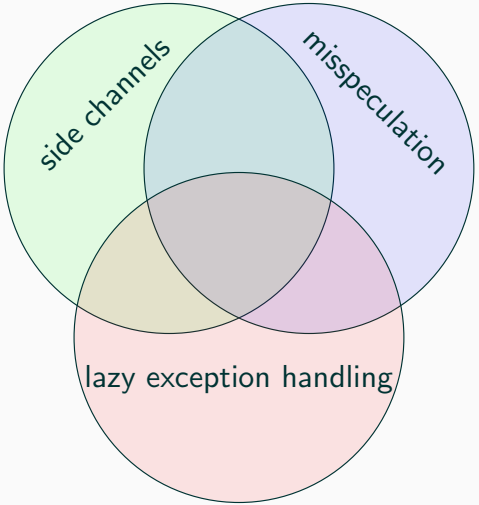

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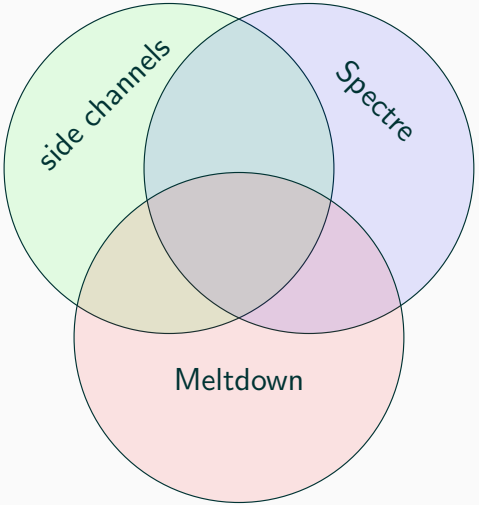

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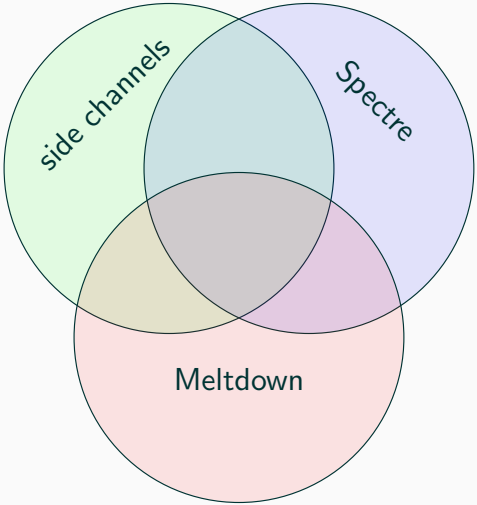
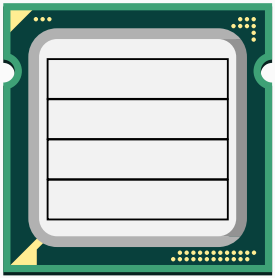
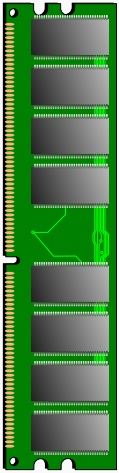


- traditional cache attacks (crypto, keys, etc)
- actual misspeculation (e.g., branch misprediction)
- Meltdown, Foreshadow, ZombieLoad, etc
- **Let's avoid the term Speculative Side Channels**

```
printf("%d", i);
printf("%d", i);
```





CPU Cache

```
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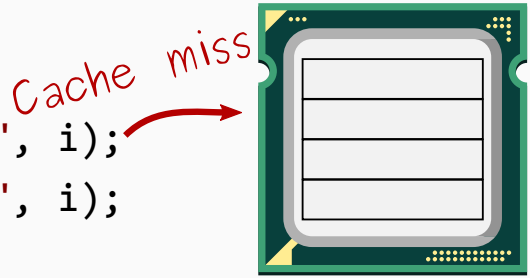

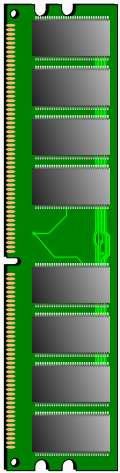

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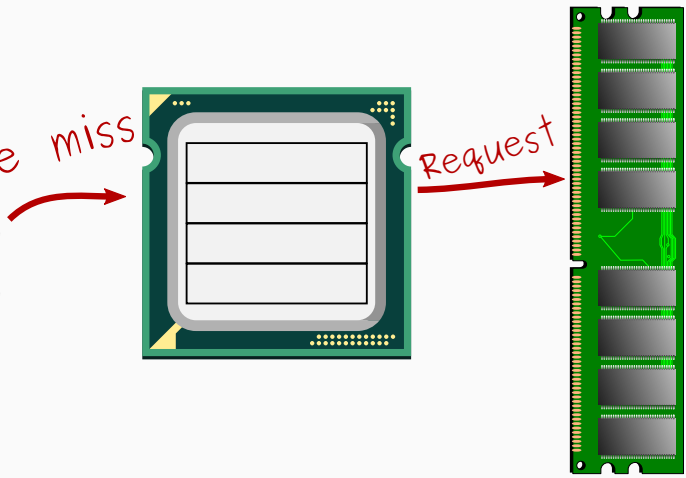

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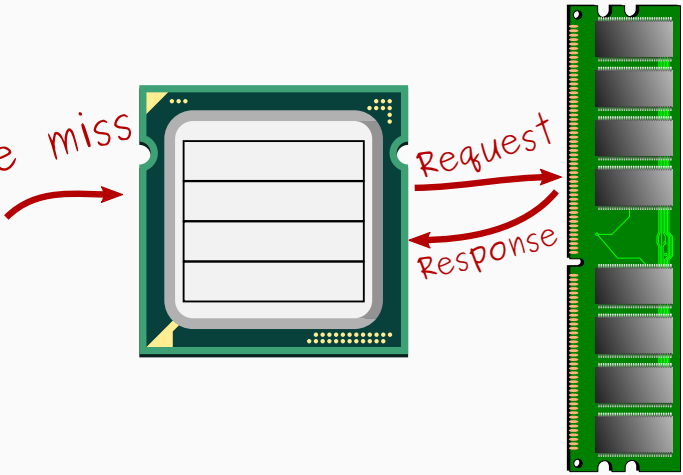

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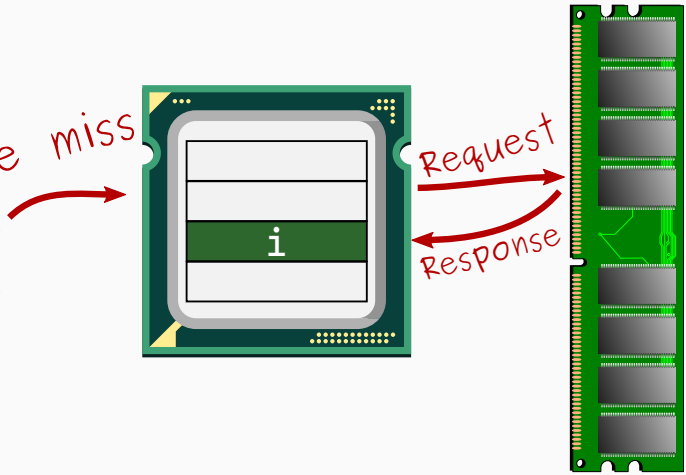
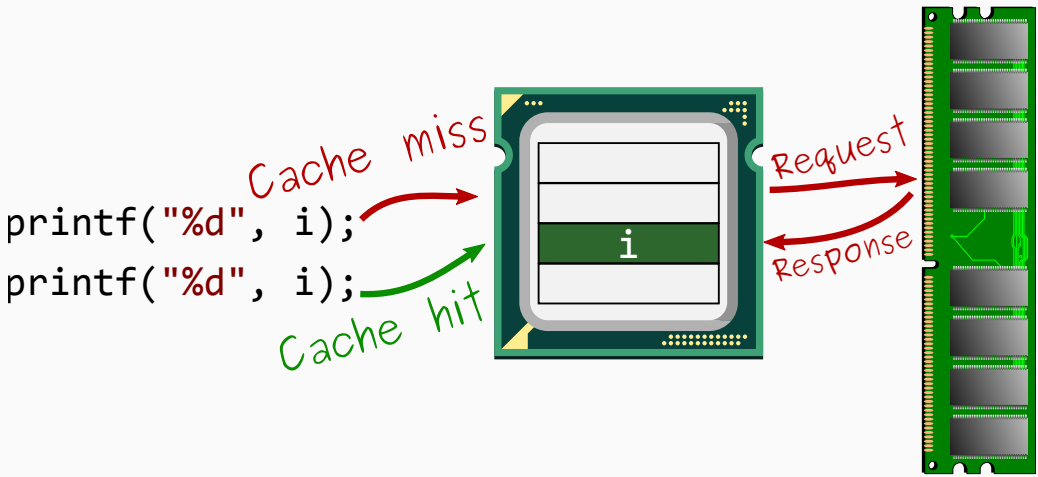
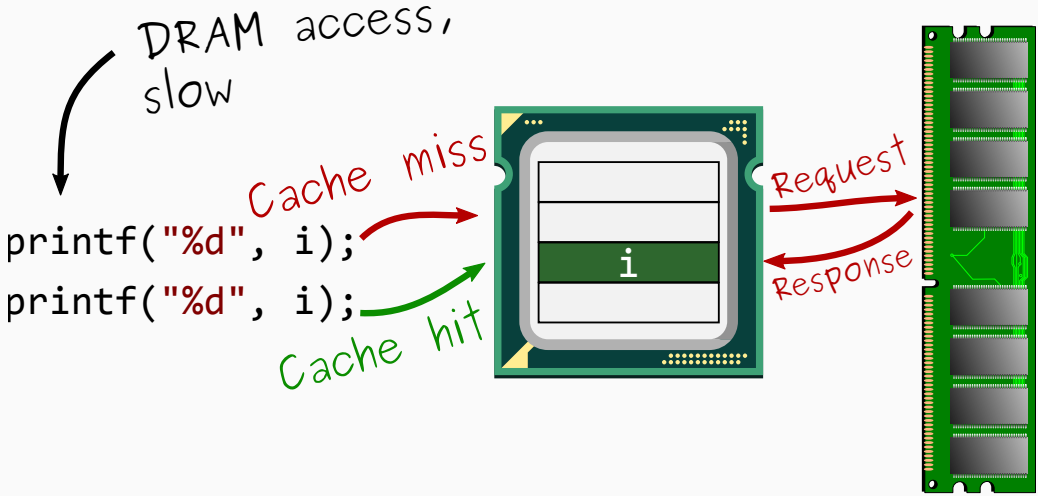



printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response


DRAM access, slow
printf("%d", i);
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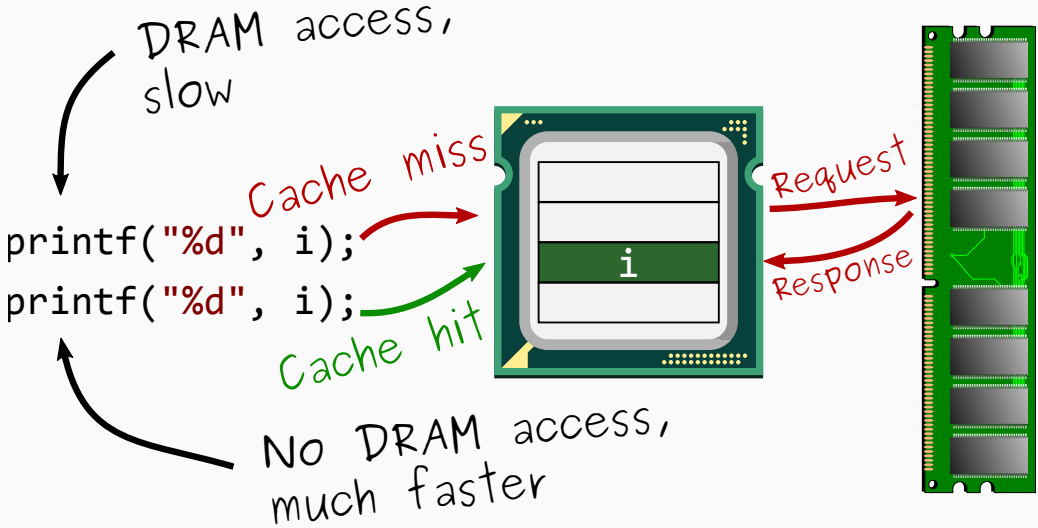
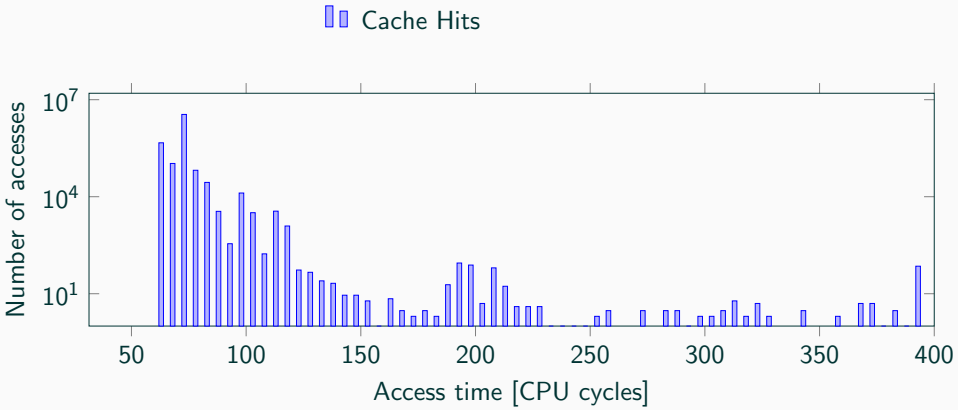
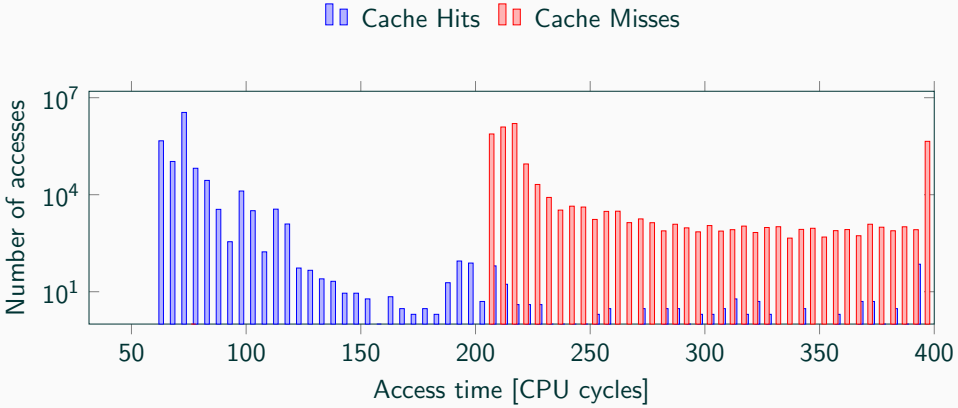
Cache hit
i
Request
Response

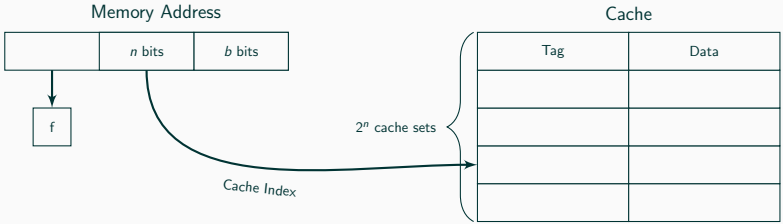

DRAM access, slow
printf("%d", i);
printf("%d", i);
Cache miss
Cache hit
i
Request
Response
No DRAM access, much faster

Memory Access Latency




Cache Hits
Cache Misses
Number of accesses
10^7
10^4
10^1
50
100
150
200
250
300
350
400
Access time [CPU cycles]

2-way set associativity



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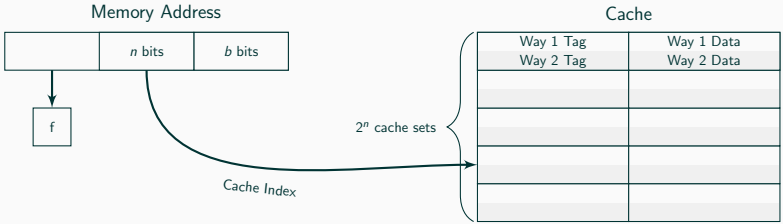

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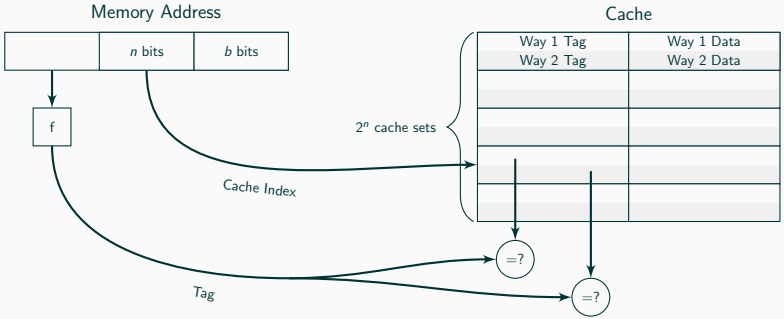

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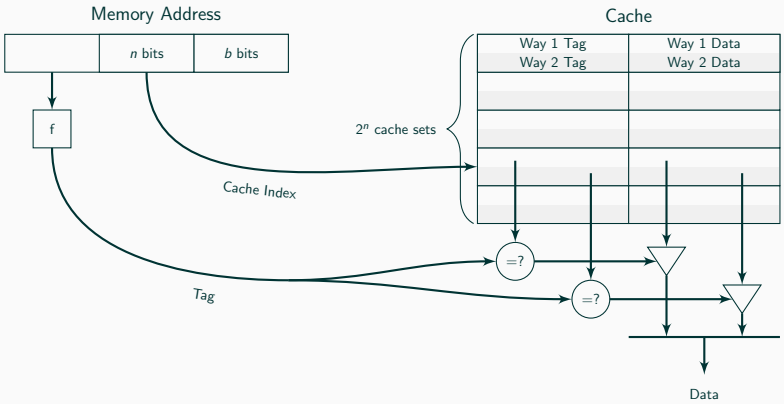
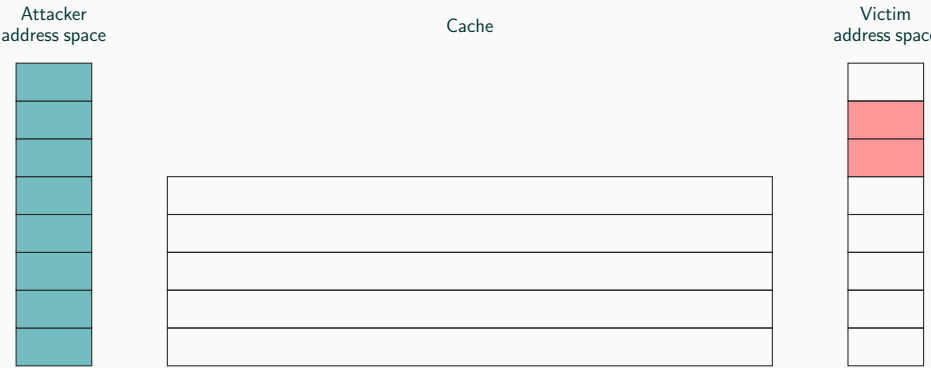
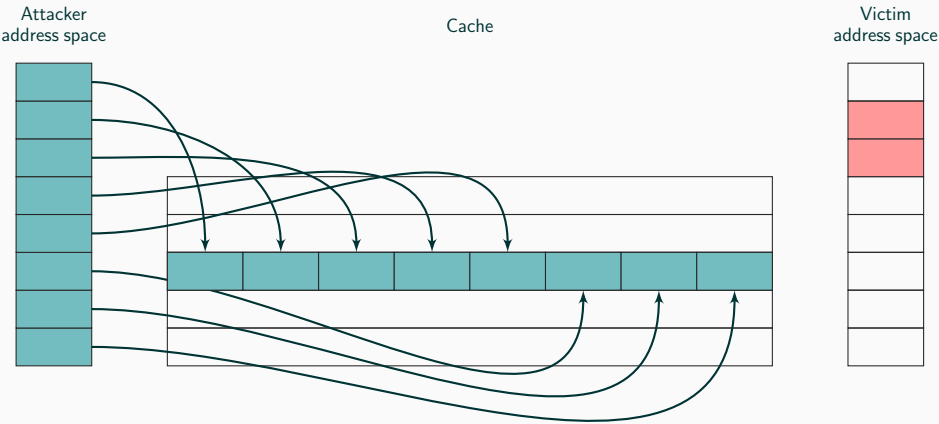



Attacker
address space
Cache
Victim
address space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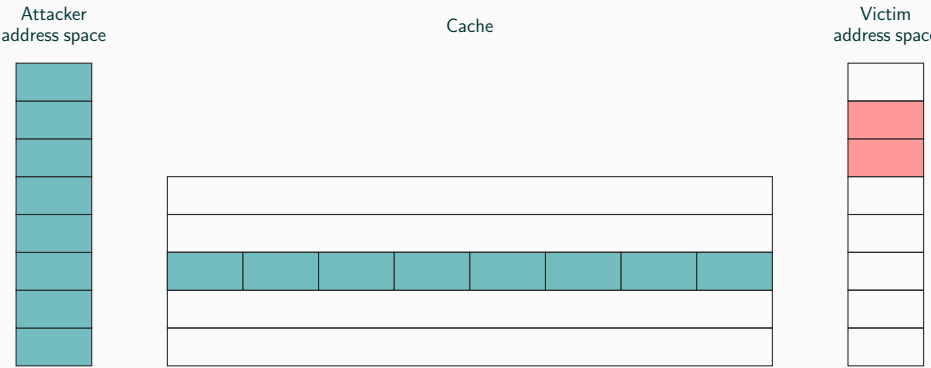
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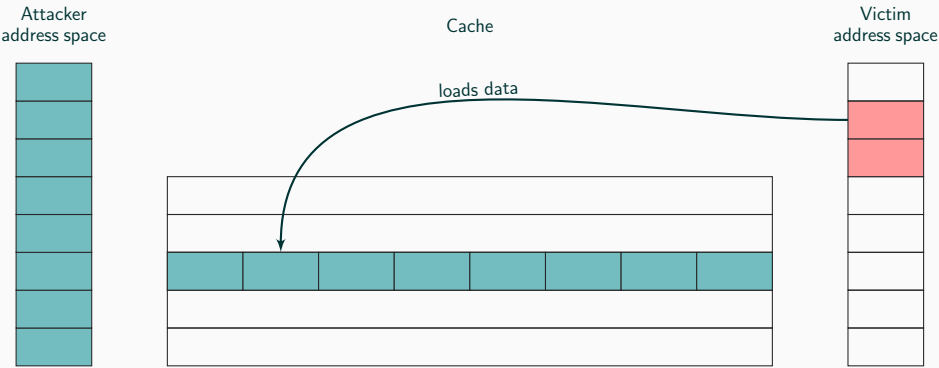
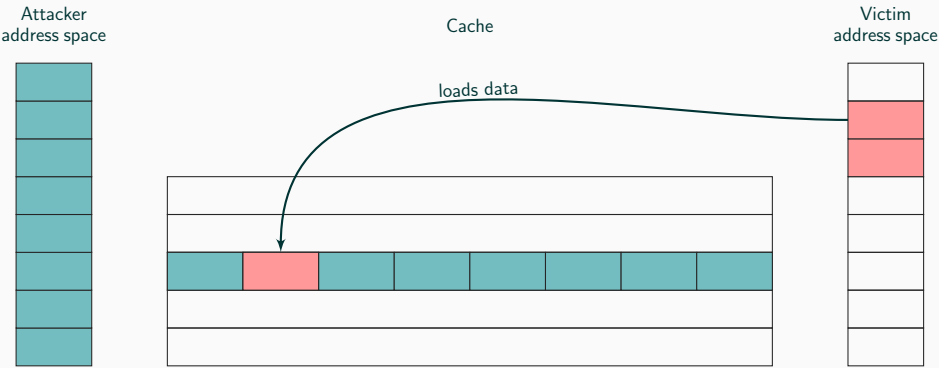
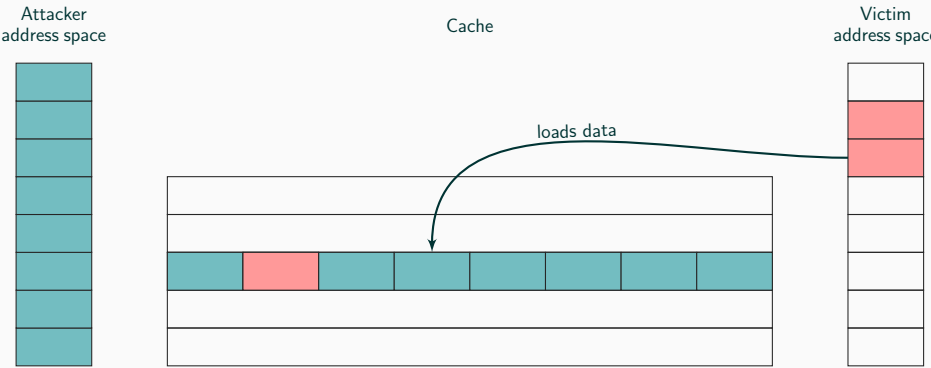
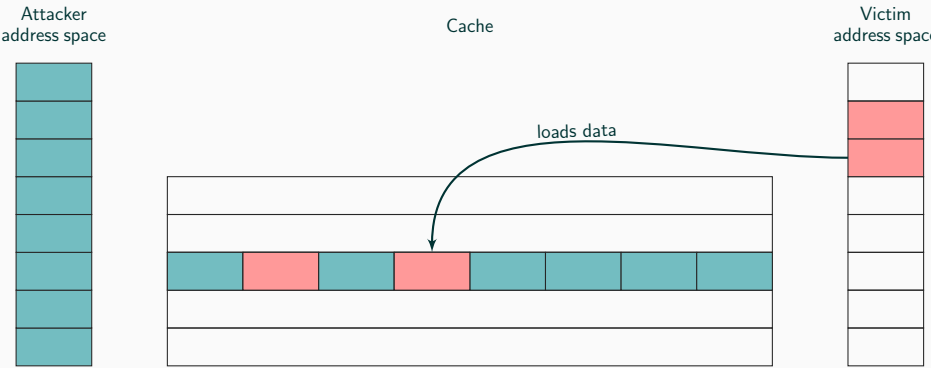
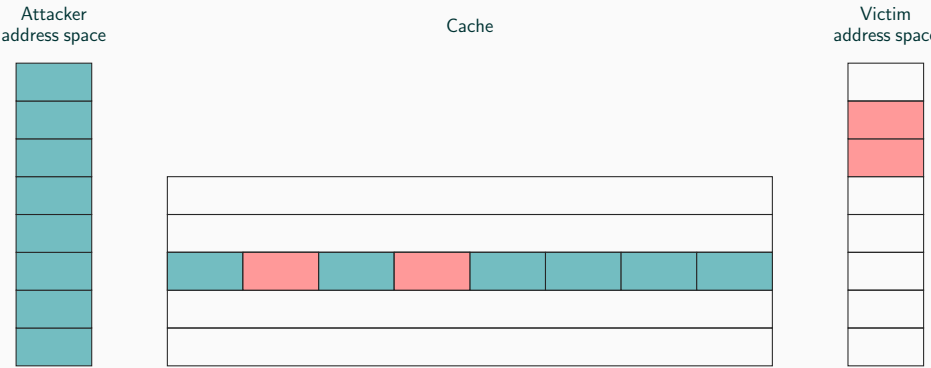
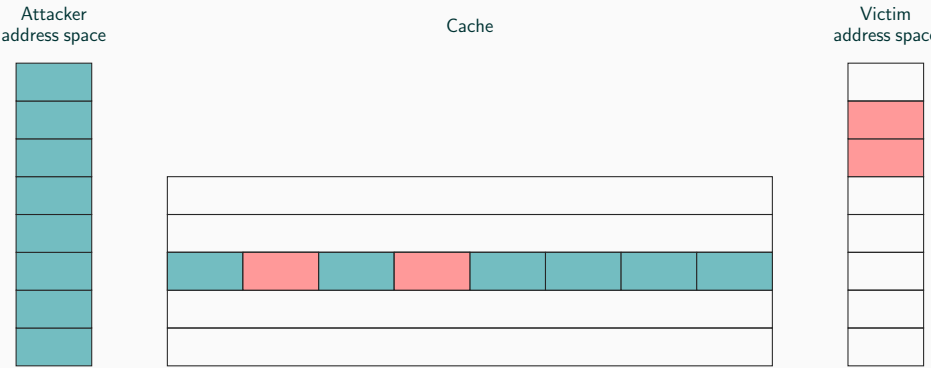

Attacker
address space
Cache
Victim
address space
loads data

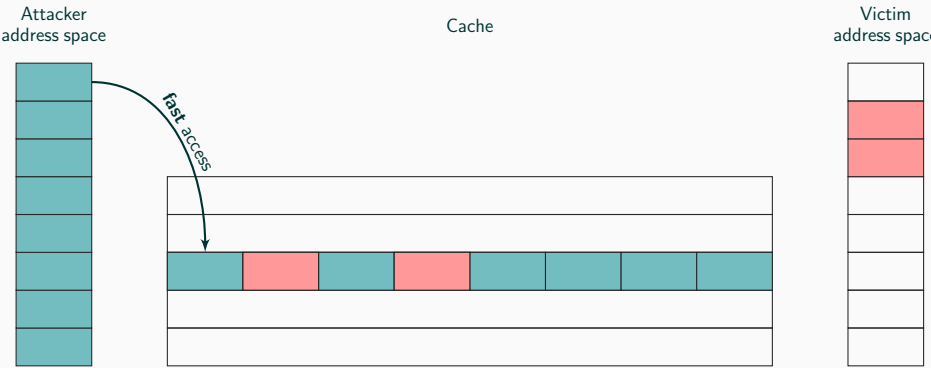

Attacker
address space
Cache
Victim
address space
loads data

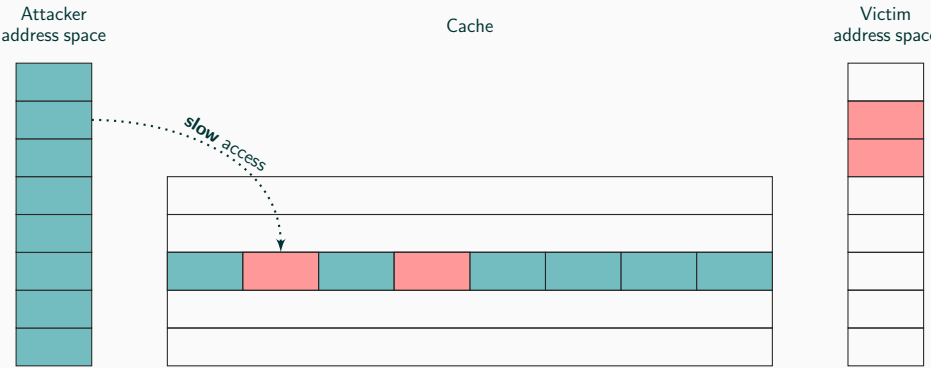

Attacker
address space
Cache
Victim
address space
loads data


Attacker
address space
Cache
Victim
address space
loads data


Attacker
address space
Cache
Victim
address space


Attacker
address space
Cache
Victim
address space


Attacker
address space
Cache
Victim
address space
fast access


Attacker
address space
Cache
Victim
address space
slow access

ScatterCache

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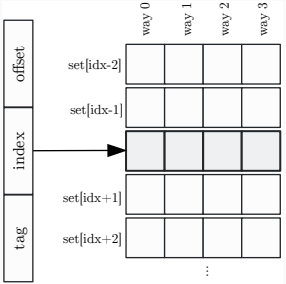
instead of this:



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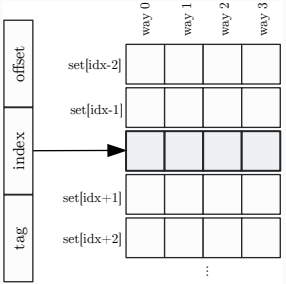
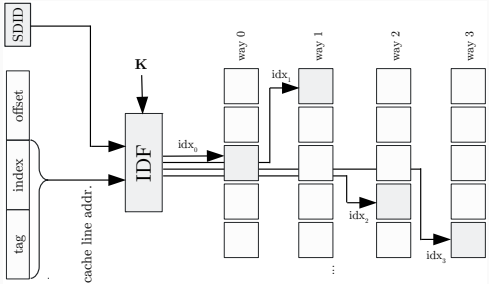
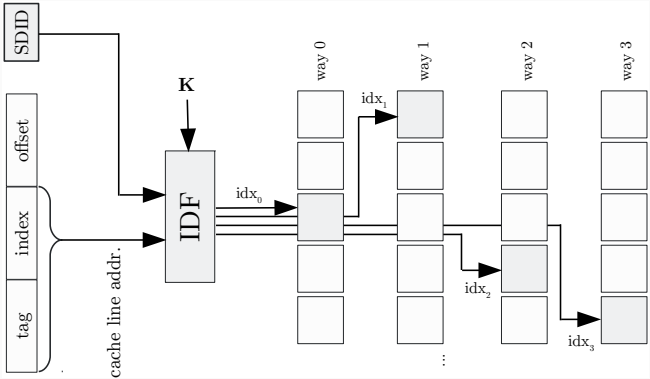
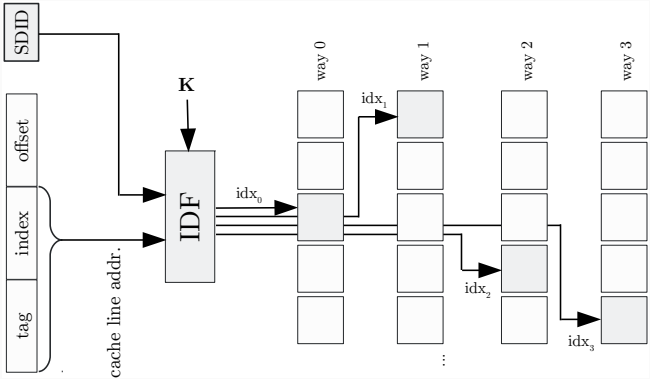


let's do this:





- Index Derivation Function (IDF) takes an address and returns a cache set



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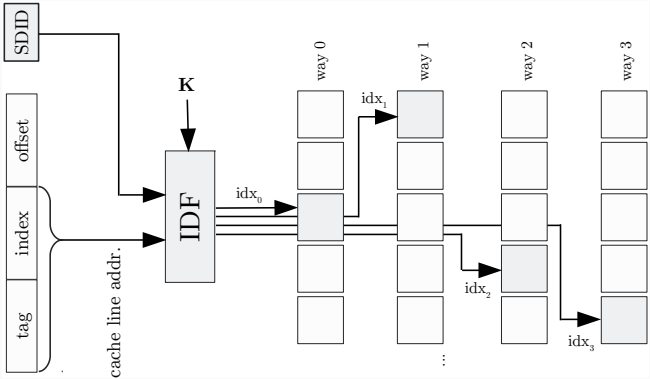
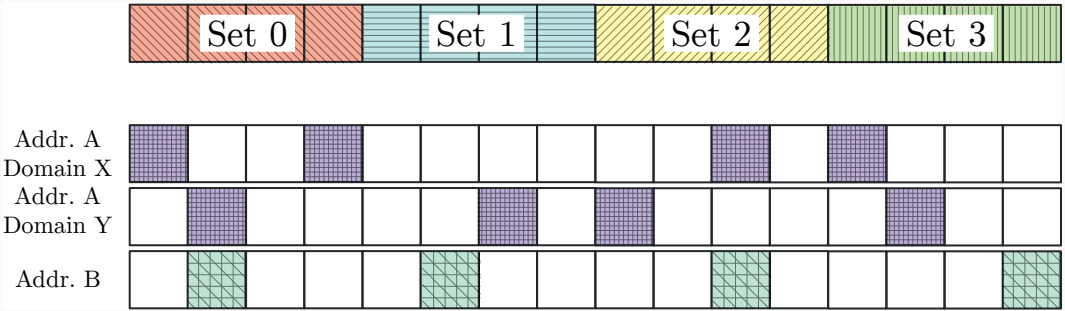


- Index Derivation Function (IDF) takes an address and returns a cache set
- Depends on hardware key K and optional Security Domain ID (SDID)
- → unique combination of cache lines for each address


Set 0
Set 1
Set 2
Set 3
Addr. A
Domain X
Addr. A
Domain Y
Addr. B

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- But - OS support enables security domains
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- OS can define SDID per process and separate user space and kernel space
- Process can request distinct SDIDs for memory ranges

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- Shared, writable memory can't be separated, eviction-based attacks are hindered

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- Constructing this set requires $\approx 2^{25}$ profiled victim accesses, compared to less than 100 accesses for standard, noise-free Prime+Probe

- Micro benchmarks GAP, MiBench, Imbench, scimark2 on gem5 full system simulator

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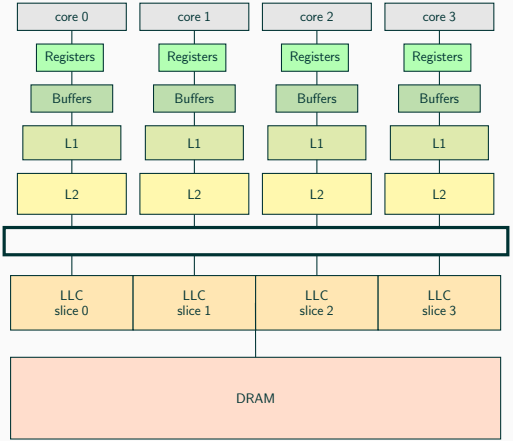
- Cache hit rate always at or above levels of set-associative cache with random replacement
- Typically $2\% - 4\%$ below LRU on micro benchmarks, $0\% - 2\%$ for SPEC

ConTExT

Where can data be?



ConTExT Idea

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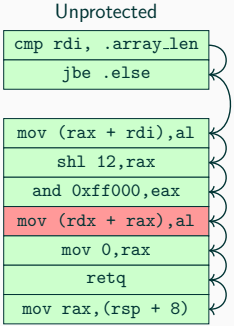
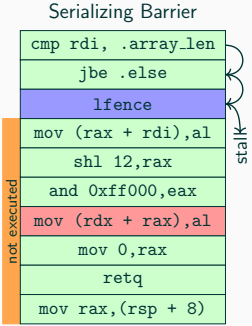
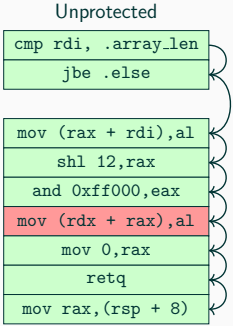

Unprotected
cmp rdi, .array_len
jbe .else
mov (rax + rdi),al
shl 12,rax
and 0xff000,eax
mov (rdx + rax),al
mov 0,rax
retq
mov rax,(rsp + 8)

ConTExT Comparison





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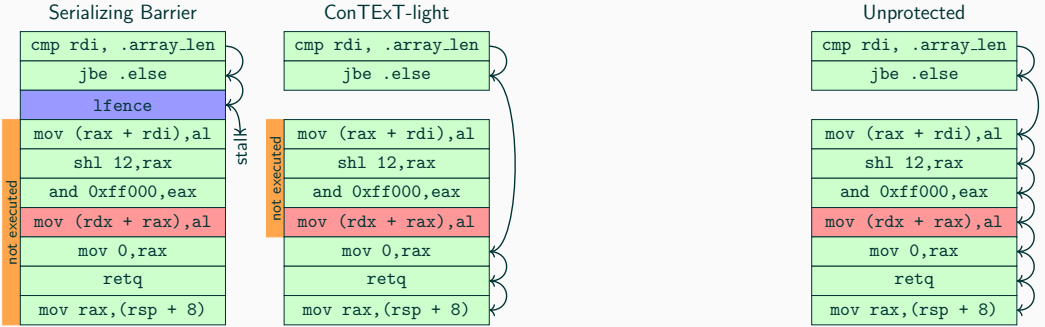

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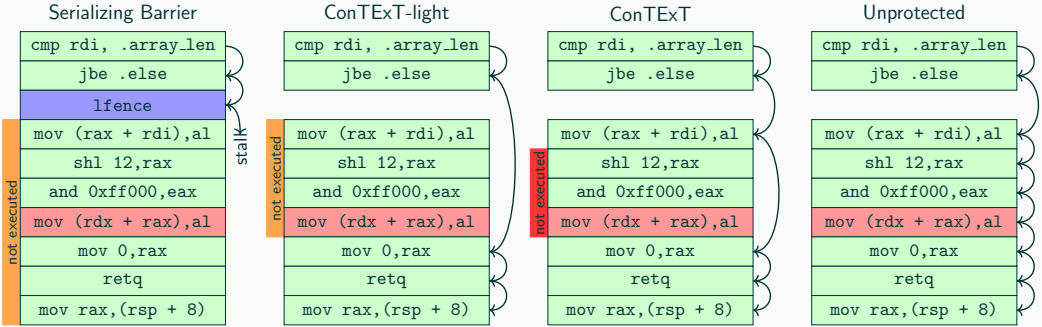

Avoiding Taint Explosion

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- Split stack into protected and unprotected half

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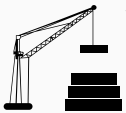
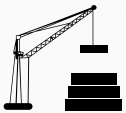
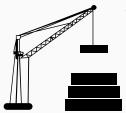
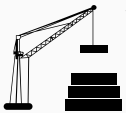
  $\rightarrow$ Untaint register
- Split stack into protected and unprotected half
- Stack spills of unprotected data $\rightarrow$ stay unprotected as long as they stay in the cache







- Compiler Extension



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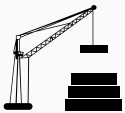

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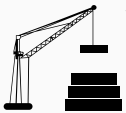

- Compiler Extension
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- Native via uncacheable memory (ConTExT-light)

Benchmark	SPEC Score		Overhead
	Baseline	ConTExT	[%]
600.perlbench_s	7.03	6.86	+2.42
602.gcc_s	11.90	11.80	+0.84
605.mcf_s	9.06	9.16	−1.10
620.omnetpp_s	5.07	4.81	+5.13
623.xalancbmk_s	6.06	5.95	+1.82
625.x264_s	9.25	9.25	0.00
631.deepsjeng_s	5.26	5.22	+0.76
641.leela_s	4.71	4.64	+1.48
648.exchange2_s	*would require Fortran runtime*		
657.xz_s	12.10	12.10	0.00
Average			+1.26

Table 1: Performance of the ConTExT split stack using the SPECspeed 2017 integer benchmark.

DRAM organization

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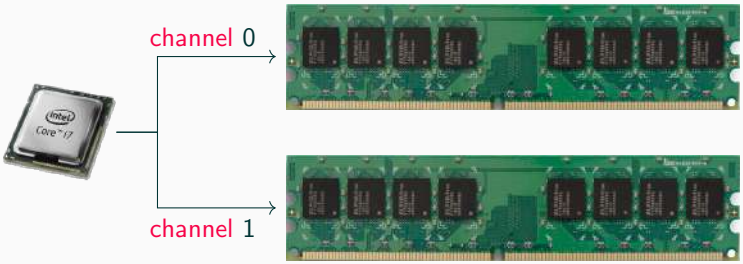
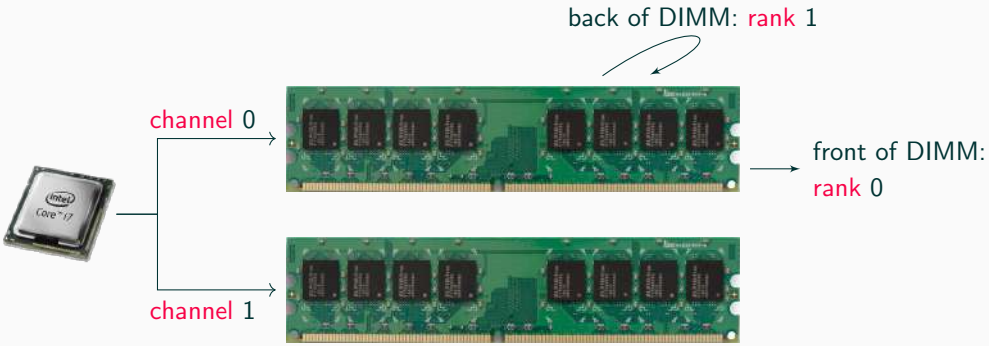
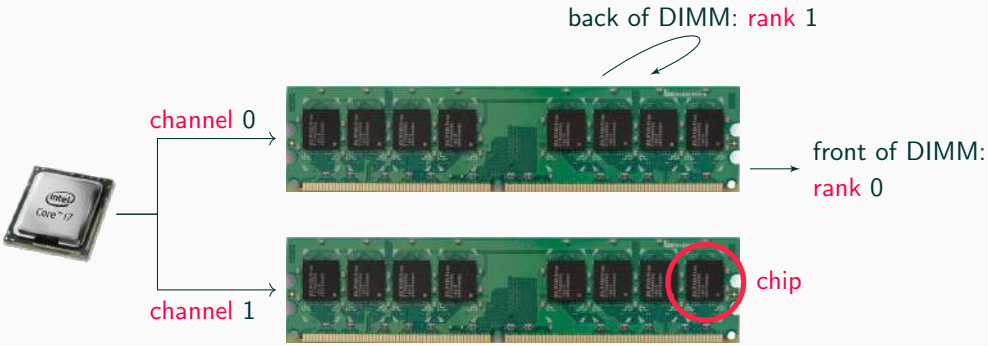



back of DIMM: rank 1
channel 0
front of DIMM:
rank 0
channel 1


back of DIMM: rank 1
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DRAM organization

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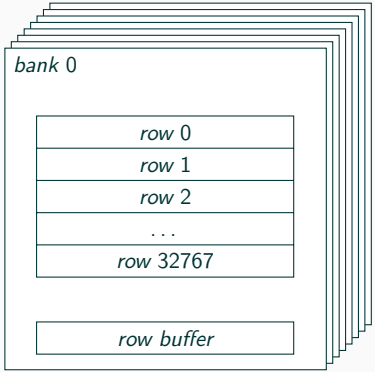
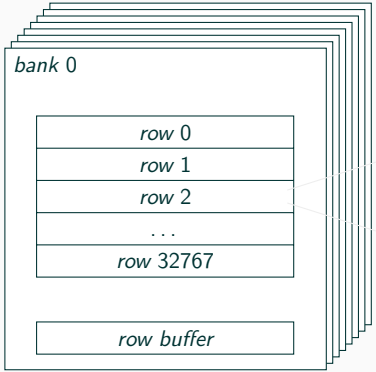
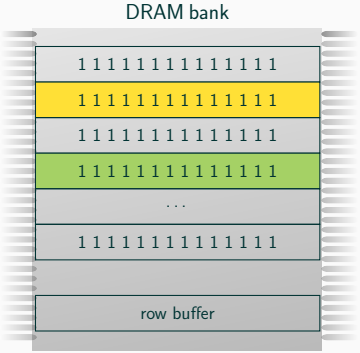


DRAM organization

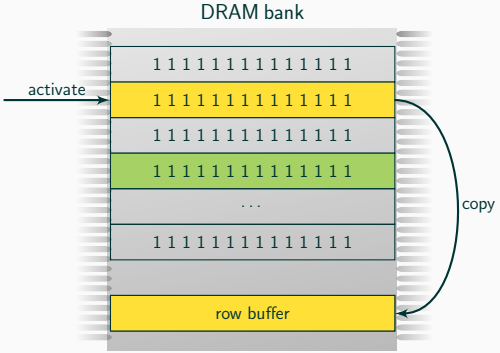
chip



64k cells
1 capacitor,
1 transitor each



- Cells leak → repetitive refresh necessary
- Maximum interval between refreshes to guarantee data integrity
- Cells leak faster upon proximate accesses → Rowhammer



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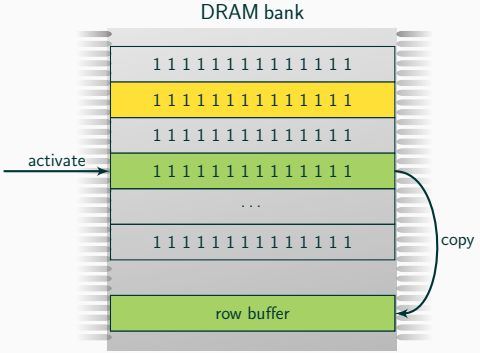

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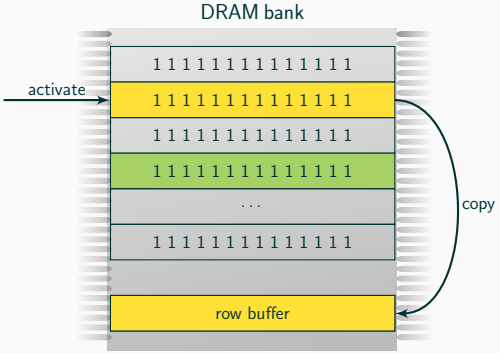

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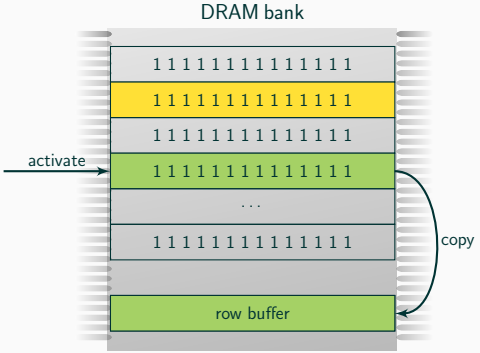

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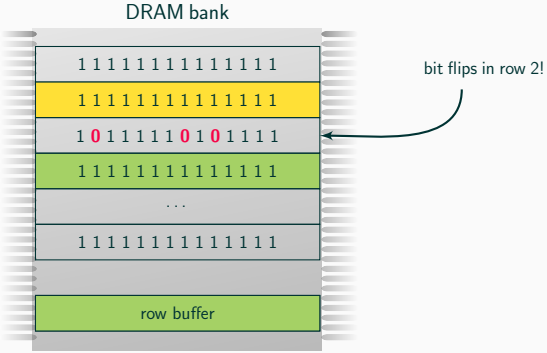

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Quick fixes (that don't work)

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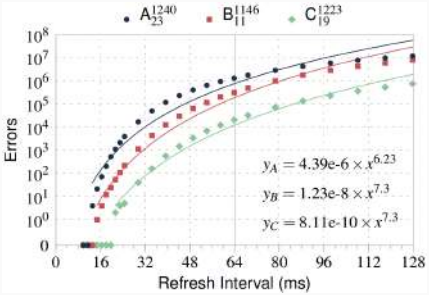

Errors depending on refresh interval

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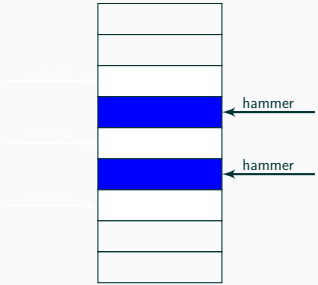
- for $p = 0.001$ and $N_{th} = 100K$, experiencing one error in one year has a probability 9.4×10^{-14}

Target Row Refresh (TRR)

- counter per row
- increment neighbor rows
- refresh when counter reaches a threshold



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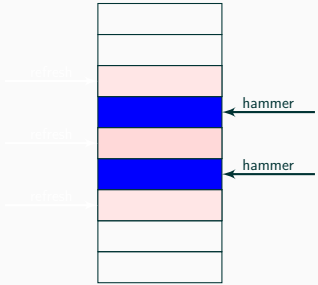

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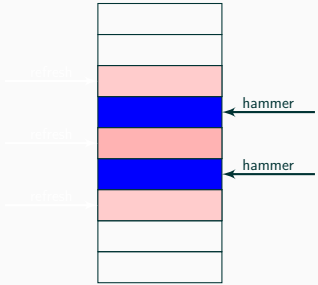

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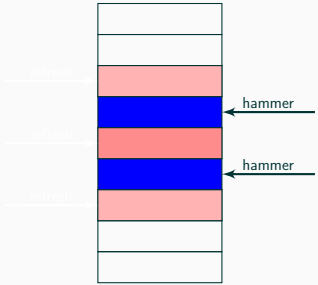

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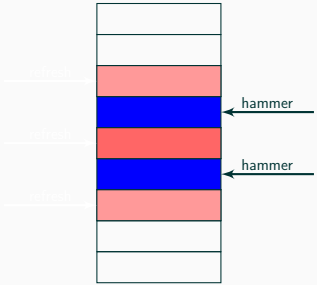

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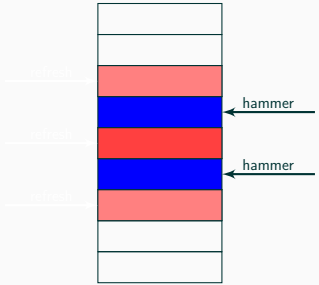

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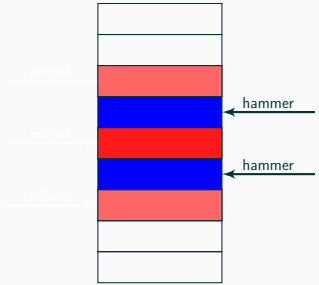

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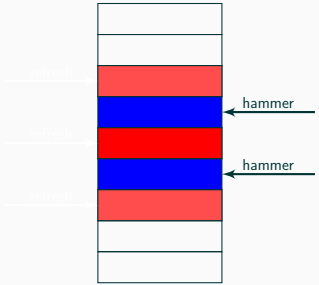

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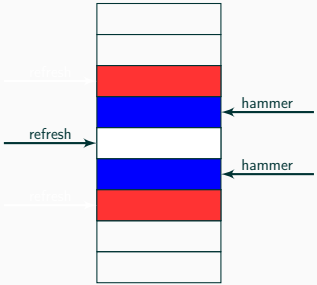

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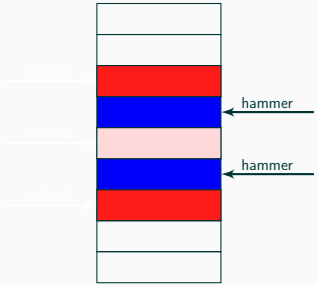

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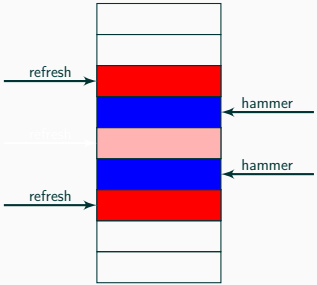

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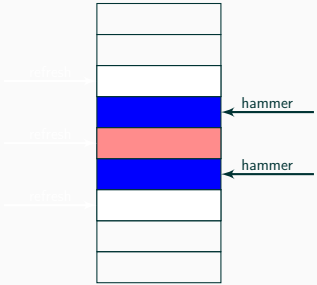
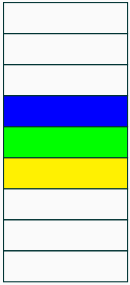


- B-CATT: disable vulnerable physical memory
- G-CATT/ZebRAM: isolate security domains in physical memory

B-CATT/ZebRAM

G-CATT



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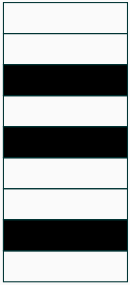

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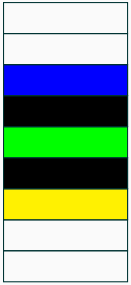

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Papers co-funded by ARM

C. Canella, J. Van Bulck, M. Schwarz, M. Lipp, B. von Berg, P. Ortner, F. Piessens, D. Evtyushkin, and D. Gruss. A Systematic Evaluation of Transient Execution Attacks and Defenses. In: USENIX Security Symposium. 2019.

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Conclusions

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- important to distinguish between different attacks

Mitigation Plans for Microarchitectural Attacks

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